Applicability of Superconducting Interconnection Technology for High Speed ICs and Systems

Final Report/Quarterly Report
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SECTION I

FINAL REPORT

Final Report

1.1. Introduction/Summary

The studies and analysis discussed in the quarterly reports on the program (Sections 2 and 3) indicate that there are strong advantages for the use of high temperature superconductors for the signal interconnections in large, very high density 2-dimensional multi-chip modules of the types illustrated in Fig 1-1. MCMs is described in detail in Section 3.1, an analysis of the number of signal interconnect layers versus MCM size for maximal density (surface "tiled" width IC chips with minimal spacing between them) square MCMs. The comparison, between room temperature copper and HTSC interconnect materials, is based on a number of assumptions described in detail in that section. The assumptions include: 1) chip I/O counts determined from Rent's rule as published by IBM for high performance chips (eg. 370 I/O's for a 10,000 gate chip, taken to be 0.6 cm square), 2) average wire lengths from Donath model with Rent's rule exponent of p = 2/3, 3) a conductor width of W, a thickness of W/2 and spacing of 3W, where W is the same for all conductors and selected to meet line resistance limitations, 4) a 40% utilization of theoretical channel space by actual interconnects (40% wiring efficiency), 5) the longest line does not exceed two times the MCM size (ie., corner to corner line with "Manhattan" wiring with no "wrong way" routing, 6) both the dc and 300 MHz ac (eg; 3rd harmonic of a 100 MHz clock; copper skin effect losses get worse as the square root of frequency), 7) a room temperature bulk resistivity (1.68 μ Ω-cm) value is assumed, and 8) a maximum allowable resistance for the worst case line of 10 ohms (adequately small in comparison to the characteristic impedance for either load-terminated or source-terminated interconnects).

Maximal-Density HTSC MCM "System on a Substrate"

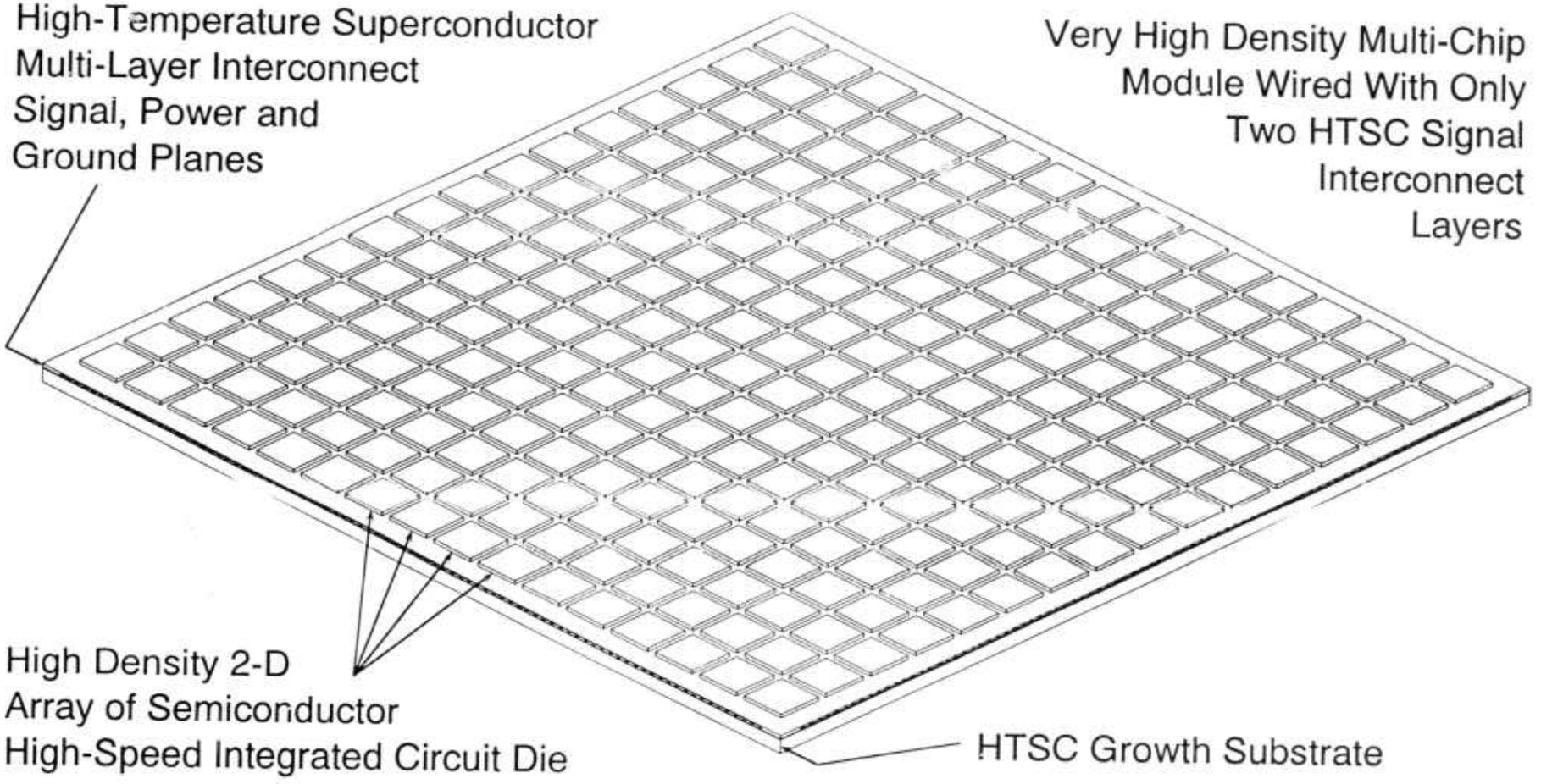


Figure 1-1

As described in the text, the analysis indicates that under these assumptions, a 6-inch square MCM tiled with 10K gate chips mounted on a 0.635 cm pitch would hold 576 chips (24 rows and columns), but would require 62 layers of room temperature copper signal lines to complete the over 100,000 interconnects between chips. With the usual triplate configuration (one layer of X and one layer of Y direction signal lines sandwiched between pairs of ground [reference] planes), the total number of metal (including ground) layers would be 93! While IBM uses 63 layers for their Enterprise System 9000 modules, these have available a full set of "E-C" (engineering change) pads on the surface with which patch and repair strategies can be executed. (These, of course, greatly reduce the number of chips that can be mounted on the MCM - eg., 121 for the 5" IBM boards). Creating defect-free boards with 93 metal layers would appear, from a manufacturing standpoint, highly un-feasible, to say the least.

With high temperature superconducting interconnects, on the other hand, this same maximal density 6" MCM can be wired using only 2 levels of signal interconnects (one "X" and one "Y"). This is possible by reducing the width of the signal lines to levels (eg., W or $\approx$ 1.5 μm$-$2μm) limited by photolithography rather than line resistance (W or $\approx$ 50 μm for copper). Obviously, even with only two signal interconnect layers it will not be easy to make the 1.5 miles of signal lines on a 6" MCM completely free of defects, but with only one X and one Y layer of lines, it should be practical to develop laser or other repair strategies to handle modest numbers of defects after completion of the boards.

The attraction of the HTSC interconnect MCM, then, is that large "system on a substrate" sized maximal density MCMs could be simply manufactured with only two signal layers (using board repair strategies to deal with material and processing defects). The payoff for putting everything in the same 1st-level (MCM) package is avoiding the large inter-package delays involved in passing through the second level (eg., circuit board level) of packaging when the IC chips must be divided among many MCMs. Since usually the interconnect delays are not more than 25% to 40% of the cycle time, simply reducing interconnect delays without corresponding reductions in the logic delays in the ICs would not buy that much in the way of system

performance. (In principle, however, sharply reducing the required total MCM area and the number of MCMs [typically to only one], and largely eliminating a whole level of packaging, should be capable of sharply reducing system costs [offset to some degree by the cost of cryogenic cooling]). In fact, however, suitably designed IC chips have much shorter logic delays when operated at liquid nitrogen (77°K) temperature than when operated at room temperature (2X to 3X faster for CMOS is frequently cited). Hence, by shortening both the logic delay (which taken by itself would not be too effective if the interconnect delay were not changed) and at the same time reducing the interconnect delay (by mounting everything on a single maximal density MCM), adoption of the HTSC MCM approach could lead to up to 3X speed improvements at the system level. Remembering that if the speed of a $1M machine is increased 3X it is worth at least $3M (sometimes much more than that), it would appear that there is plenty of value margin to pay for the cost and inconvenience of having to do cryogenic cooling.

Having established the motivation for undertaking HTSC MCM development, the next question to address is whether it is possible to make maximal density HTSC MCMs. As is noted at length in Section 3.2, because the digital pulse signal currents are typically of the order of 20mA, with a line width of only 1.5 to 2μm , the signal current densities ($J_s \approx 10^6$ A/cm^2) and induced magnetic field densities (~ 100 Gauss) are high (though within the ranges demonstrated for high quality HTSC MCM materials at 77°K), necessitating the use of top quality HTSC films for the signal lines. Such quality levels are currently obtained in highly oriented (essentially epitaxial) HTSC films. As shown in Fig 1-2, even the simplest practical HTSC MCM structures require at least 4 HTSC layers, separated by optimized dielectric constant insulator layers. These HTSC materials such as YBCO and "Thallium" are complex structured ceramics, very carefully prepared to obtain high performance. This is a far, far cry from the simple organic or amorphous dielectrics and evaporated, sputtered or plated metal interconnect lines used in conventional MCMs. Obviously, substantial advancements in the art and technology of HTSC materials growth and processing will be required to make HTSC MCMs. In particular, preparation of HTSC layers for signal lines on relatively low dielectric constant insulating materials will be required in order that the signal propagation velocities

(which vary as $\varepsilon_r^{-0.5}$) not be compromised. Fortunately, as shown in Fig.1-2, it is possible to grow the first 3 layers of the HTSC MCM structure (power, high ε_r thin dielectric, ground, low ε_r thick dielectric and the first signal plane) "in-situ" (ie., without removing from growth system). The signal line must be patterned and the next low dielectric constant layer deposited (and planarized if necessary) before the top signal interconnect HTSC layer is grown and patterned. Note that the use of a thin (~ 1000 A° or so) $SrTiO_3$ layer ($\varepsilon_r \approx 1000$) between the power and ground planes will give a power supply bypassing of about $1\mu F/cm^2$, which is an enormous advantage. Because there is no need (or really desire) to have the line resistance be zero (under 10Ω for the longest lines will suffice), the vis and pad layers can be normal metals as long as the quality of the small area contacts to the HTSC layers is good. (Jack Ekin at NIST, Boulder has made $2\mu m \times 2\mu m$ contacts to YBCO which handle at least 30mA with only 30 milliohms resistance, so this seems do-able.) As shown in Fig. 1-2, such inter-layer vias can be processed last by "going over the top" with the final, pad layer of normal metal (presumably repairs after completion can be done in the same way). Hence it appears that HTSC MCMs can be realized by fairly straightforward structures, though the actual technology development work might lead to functionally equivalent structures quite different from Fig. 1-2. In any event, the demands on the HTSC growth and processing technologies will be severe. Table 1-1 reviews many of the demands on the HTSC technology for this ultra high density MCM application.

Assuming that a viable HTSC MCM technology can be realized as a new advanced packaging technology (and the probability that this can be done appears to be getting better all the time), how would it fit in with more conventional and alternative advanced packaging approaches in the world of MCM system applications? Table 1-2 gives an overview of this comparison. Normal metal interconnect technologies include both the "conventional" 2 to 6 signal layer inexpensive MCMs (as manufactured, for example, by n-CHIP) and the "exotic" 10 to 40 signal layer MCMs (like the IBM Enterprise System 9000 MCMs mentioned previously). Conventional metals will also be used (at least initially) for the signal interconnects in the diamond substrate 3-dimensional interconnected advanced

Example of Simple HTSC MCM Cross-Section

R. C. Eden 10/91

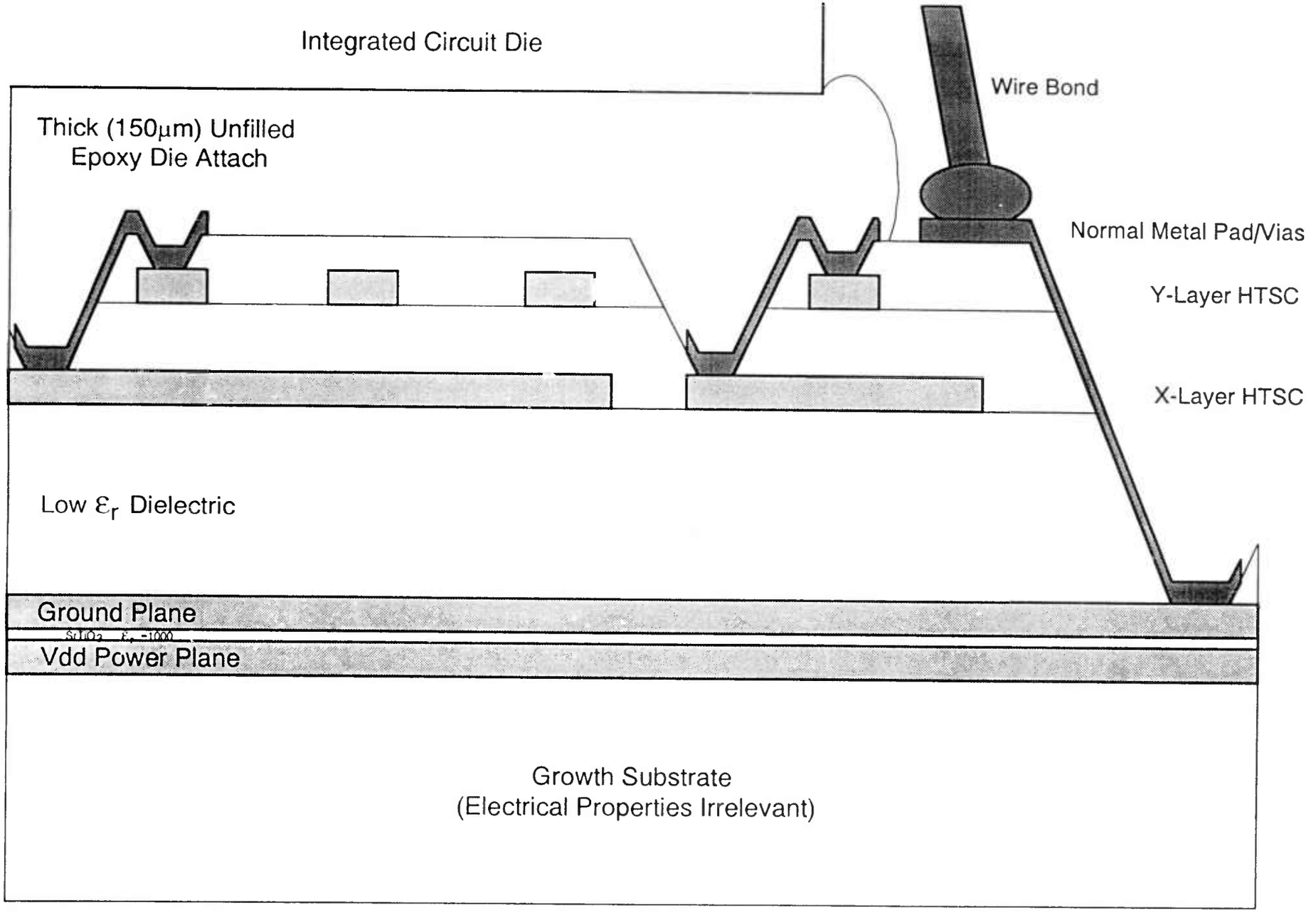


Figure 1-2

Requirements For Digital MCM Application For HTSC Interconnects

1)	Substrate Size	Large: 2" Entry Level, 4" to 8" For Biggest Advantage.
2)	Number Of HTSC Layers	4 Total: 2 (One X, One Y) Signal Interconnect, Ground, Power (Interplane VIA Interconnects, Pad Layers, Etc. Can Be Normal Metal).
3)	Interlayer Dielectrics And Their Dielectric Constants	All May Need To Be Epitaxial To Support HTSC Growth Signal Conductor Require Low Dielectric Constant ($\varepsilon_R \approx$ 4 to 9 or less) Thin, Very High ε_R Dielectric Required Between Power And Ground.
4)	Signal Interconnect Linewidths And Thicknesses	W $\approx$ 1.5μmto 3μmon 6 to 10μm Pitch With Good Linewidth ControlThickness Of 0.5μm to 1μm For Low B-Field And Normal Reistance.
5)	Signal Current Densities And B-Fields	$I_{SIG} \approx$ 20mA Gives $J_{SIG} \approx$ 1 x 10^6 to 2.5 x 10^6 A/cm^2 For 1.5μm To 3μmLines Signal B-Fields $\approx$ 100 GAUSS At Conductor Surface.
6)	Required Signal Fidelity (Conductor Loss, R_S, Etc.)	$\approx$ 10% Leading Edge Loss (Undershoot) Generally Acceptable For Full Amplitude ($\approx$ 1V to 3V) Pulses Of $T_R \approx$ 50ps to 1ns For 8" to 16" Lines or $R_S \approx 5 \times 10^{-5}\ \Omega$ at f = 400MHz TO 8GHz.
7)	Total Signal Line Resistances Including HTSC Defects, Normal Metal VIAs And Line Segments	10 OHMS Total End To End With Typical Dozen Or So Normal Metal VIAs in Lines.
8)	Yield / Repairability	Very High Yields Of Fineline Signal Interconnects Req'd As 4" MCM Migh Have $\approx$ 1Mile Of Signal Lines On It. Post - Process Repair Techniques Potenitally Acceptable.
9)	HTSC Operating Temperature	80°K At Best, Some Configuraions Might Run Up To 90°K Unless Improved Cooling Schemes Used.

Table 1-1

Normal Metal		Superconducting	Diamond 3-D
Operating Temperature:	≈ 300° K Typical	≈ **80° K**	≈ 300° K Typical
Size:	3" Conventional 5" Exotic	6" To 8" Board Size	4" x 4" x 4" Typical
# Of Signal Intct Layers:	2-6 Coventional 10-40 Exotic	**2** Signal Interconnect Layers	For ≈ 50 Boards 2-6 Layers/Board
# Die:	20-40 Conventional 100-200 Exotic	**500/1000** Die/Board	1000-3000 Die/3-D Module
Cost:	Conventional - Cheapest Exotic - **Very** Expensive	Reasonably **Low Cost**	More Expensive
Speed:	Depends On IC Technology And Inter-MCM Prop Delays	Fast: ≈ 3x Room Temp Speeds	**Fastest**
IC Technologies Supported:	Any	CMOS, GAAs Now Si-Ge ECL Or BICMOS Future	Any
Power Handling:	Depends On Package Details, Can Be High.	Medium To Low Power (Because Of Cooling Overhead)	**High Power** OK (eg. up to 20 KW - 40KW/Module
MCM Application Areas:	Low - Medium Performances, Room Temperature	High Performance, Very **Cost Effective**	**Highest Performance** And Volume Density (Highest Clock Rate Capability)

Table 1-2

MCM packaging technology. In this approach, many thousands of vertical interconnects are distributed over the areas of typically 4" x 4" diamond substrate MCM boards which have large numbers of vertical vias through them, permitting arbitrary high density X - Y - Z routing of signals in the stack of boards. With a vertical stacking pitch of the boards of 2mm, there might typically be 50 boards in a 4" x 4" x 4" cube module. (The incredibly high thermal conductivity of diamond is used to conductively extract the heat generated by the logic chips from the 3-D module.) Because the interconnect distances between chips are so short in 3-D, this technology is expected to be the speed champion, and it can support up to several thousand VLSI chips per module. On the other hand, the large number of vertical interconnections and vias required for 3-D will be more costly than if the requisite number of chips can be packed on one 2-D substrate.

The HTSC MCM technology represents a very cost effective approach to achieving almost diamond 3-D levels of performance and numbers of VLSI chips in a very simple, straightforward way (given that the HTSC boards can be manufactured and convenient cryogenic coolers developed). HTSC MCM boards require only 2 levels of signal interconnects which should make testing and debugging, as well as bare board repair), fairly easy. HTSC MCMs of the order of 6" to 8" (150mm to 200mm) on a side should hold 500 to 1000 VLSI die. While only CMOS or GaAs chips currently function properly at 80°K, in the future, Si - Ge "strained layer" heteroepitaxial ECL or BiCMOS technologies may also be useable. However, because of the cryogenic speed enhancement of CMOS, near-ECL speeds can be obtained with this workhorse VLSI/ULSI IC technology, enabling a very high level of system performance to be realized in a very cost effective (particularly considered on a price / performance basis) way. That is, of course, why there is so much excitement about HTSC MCMs.

1.1.1. Potential for Possible Technology Alternatives for HTSC MCMs

It is important to remember that the reason for the attractiveness of HTSC MCM packaging in terms of system performance, low cost, small size, etc., has nothing to do with the interconnects being superconducting per se. It is just the fact that the chips operate faster at 80°K and that the use of HTSC interconnects allows all of them to be placed essentially shoulder to shoulder on a single very large, very high density MCM which, because only 2 signal layers are required, should be reasonably easy to manufacture, test and repair. If by some means it were possible to invent some other new technology or combination of technologies which could duplicate this same MCM size and density (and also operate at cryogenic temperatures) and also be manufacturable, testable and repairable, then it could serve as well. Of course, these alternatives may themselves be more difficult to develop than HTSC MCMs, or have other disadvantages, but they are worth considering.

The first alternative would be copper interconnects cooled to 80°K. For pulse rise times in the 40ps to 0.4ns range, the maximum signal frequency components are in the 10^9 to 10^{10} Hz range. While room temperature copper ($\rho = 1.68\,\mu\,\Omega$-cm) has a surface resistance, R_S of 8.3 mΩ at 10^9 Hz or 26 mΩ at 10^{10} Hz, at 77°K the R_S falls to about 3.9 mΩ at 10^9 Hz or 14 mΩ at 10^{10} Hz, about a factor of 2 improvement (these are measured R_S values, not simply scaled from the ≈ 5 x reduction in resistivity from 300°K to 77°K). To keep the series resistance of a wire of width W and length L to some maximum value, R_{MAX}, we must have, from

$$R_{MAX} \approx \frac{L}{2W} R_S \qquad \text{Eq. 1}$$

(ignoring the nonuniform current distribution on the wire and the area of the sidewalls make, Eq. 1 approximate, but fairly accurate), so that the minimum width makes Eq. 1 W_{MIN} for a line is given by

$$W_{MIN} \approx \frac{L_{MAX} R_S}{2 R_{MAX}} \qquad \text{Eq. 2}$$

For example, for a 6" MCM with L_{MAX} = 12" and taking R_{MAX} = 10 Ω, W_{MIN} for 77°K copper would be W_{MIN} = 59.4 μm (2.34 mils) at 10^9 Hz or W_{MIN} = 213um μm (8.4 mils) at 10^{10} Hz.

The analysis of the number of signal layers required for a maximal density MCM discussed previously, and presented in detail in Section 3.1 assumed a very modest, 1ns signal rise time, using a 300 MHz frequency for the 300°K copper skin depth calculation. For that case, a W_{MIN} = 45.6 μm line width was required for R_{MAX} = 10 Ω on the 6" MCM, which led to the requirement for 62 signal layers or 93 total conductor layers. AT 77°K, then, for these relatively low 300 MHz frequency components (short channel CMOS at 77°K will be much faster than 1ns). the number of copper layers could be halved (to 46 total), but considering more realistic 10^9 frequency components to be necessary, it would still require about the 93 layers shown in the analysis. (The analysis was very kind to copper in assuming an effective wire periphery of 2W + 2t = 3W t for t = W/2, whereas current crowding makes Eqs. 1 and 2 [which assume a 2W periphery] actually closer to correct.) Hence, even copper cooled to 77°K requires a very large number (probably un-manufacturable number) of signal layers to create large (eg. 6") maximal density MCMs. It should also be noted that no one, in my awareness, has demonstrated that a "conventional" copper polyimide, (for example), MCM with many layers will be reliable in temperature cycling 77°K.

These signal layer requirements and their dependencies can be seen more quantitatively with a bit of analysis. For a maximum line length of L_{MAX} and assuming a line thickness of half of the width, W, with a normal metal resistivity, ρ, the minimum acceptable width to achieve an end to end resistance of R_{MAX} will be given by

$$W = \sqrt{2\rho L_{MAX} / R_{MAX}} \qquad \text{Eq. 3}$$

We note, for example, that the minimum acceptable line width, W, varies as the square root of resistivity, ρ, which is the same ρ dependence as obtained for the high frequency skin effect case of Eq. 2, due to the dependency of R_S in Eqs. 1 and 2 on ρ, given by

$$R_S = \sqrt{\pi \rho \mu_0 f} \qquad \text{Eq. 4}$$

where $\mu_0 = 4\pi \times 10^{-9}$ in centimeter units (this equation ignored the complication of anomalous skin effect which alters the low temperature R_S some what). In either case, cooling copper from 300°K to 77°K allows about a 2x reduction in W and hence 2x reduction in the number of signal layers, as was discussed above.

While the dependencies of line width and required number of signal layers on metal resistivity happens to be the same for the "dc" and "ac" (fully developed skin effect conduction) cases, this is not the case for their dependencies on R_{MAX} or L_{MAX}, which tend to be square root in nature for the "dc" case or proportional for the "ac" case. Note that in the plot of the required number of signal layers versus MCM size, above an MCM size of 3" for room temperature copper, the 300MHz ac (skin effect limited) curve rises above the "dc-only" curve. The point at which these depart (crossover between dc and fully developed skin effect curves) occurs at a length, L_e, obtained by equating Eqs. 2 and 3 for W, and substituting Eq. 4 for R_S as

$$L_{eq} \approx \frac{8\,R_{MAX}}{\pi \mu_O f} \qquad \text{Eq. 5}$$

where as usual, f is the frequency of the highest frequency components. L_{eq} here is interpreted as the approximate maximum length for which a R_{MAX} resistance line can be considered to be dc resistance dominated subject to the above geometric assumptions. (In the computer analysis, an effective wire periphery of 3W, rather than the more accurate 2W as used in Eqs. 1 or 2 was used, so that $L_{eq} \approx 18\,R_{MAX}/\pi \mu_O f$) was used instead of $L_{eq} \approx 8\,R_{MAX}/\pi \mu_O f$. Substituting in the ρ = 1.68 x 10-6 Ω - cm value for 300°K copper and f = 300MHz (and the constant 18 as used in the computer analysis), gives L_{eq} = 15.2 cm or 6", which is, of course, L_{MAX} for a 3" MCM, showing that Eq. 5 correctly gives the MCM size separation point between the "ac" and "dc-only" curves. From Eq. 5 (using the correct value of 8 for the constant), taking a more realistic $f = 10^9$ Hz, as appropriate for T_R = 0.4ns logic, the "ac" curve would pull away from the "dc-only" curve above wire lengths of only 2 cm, and the number of required layers for a 6" MCM would be about 170 signal layers (256 total) for R_{MAX} = 10Ω , or about 80 signal layers (121 total) if the copper temperature were reduced to 77°K. For really fast logic (eg. GaAs or Si-Ge ECL in the late 90's), T_R = 40 ps or $f = 10^{10}$ Hz needs to be considered. Here, cooled copper would require 286 signal layers (430 total) to achieve R_{MAX} = 10Ω in the 12" lines for maximal density MCMs. These are, of course, hopelessly large numbers requiring impractically thick "wiring mats", even if it were conceivable to yield them somehow. Hence, for higher performance logic with higher signal frequencies, copper has very serious problems in attempting to implement maximal density large MCMs.

A potential source of at least modest reduction in the number of normal metal (eg., 77°K copper) signal interconnect layers required would be to alter the chip to chip electrical interconnection scheme in such a way as to increase the allowable maximum line resistance, R_{MAX}. If R_{MAX} can be increased by some factor, then for skin-effect dominated frequencies, the number of layers can be proportionately reduced (but never below the dc resistance limit, of course). When the dc resistance

is the limitation, the number of signal layers required will drop as the reciprocal of the square root of R_{MAX}. The value of $R_{MAX} = 10\ \Omega$ was obtained, as described in more detail in Section 3.1, as the point for $Z_O = 50\ \Omega$, where dc noise margin in an internal - reference ECL - type (load terminated, as also used in GaAs) interconnection approach begins to be significantly compromised, and which gives a comparatively small loss in the leading edge amplitudes in source - terminated, open circuit load (CMOS - type) interconnect approaches. For the latter case, it is well known that if the source resistance is correspondingly reduced, a higher line resistance can be tolerated, even up to $R_{LINE} = Z_O$ for $R_{SOURCE} = 0$ if load capacitance effects are ignored. For this ideal case of $R_{MAX} = 50\Omega$ instead of $R_{MAX} = 10\ \Omega$, it would take substantially fewer numbers of signal layers to wire the MCM. While in fact here are serious problems with this approach, it is worth examining the implications for MCM wireability anyway. Because the IC driver output impedance tends to be nonlinear, and, of course, is non-zero, a realistic expectation might be that the line resistance might be able to be increased, for $Z_o = 50\ \Omega$, to 25 Ω (with a combination of IC driver impedance plus source termination resistor also equal to 25 Ω) and still maintain fairly good pulse reflection characteristics. For the 6" MCM example, the copper line width necessary to keep an $L_{MAX} = 12"$ line to a 25 Ω dc resistance would, from Eq. 3, be 20.4 μm at 300°K, or about 9.2 μm at 77°K. From Eq. 2, the required line widths for 10^9 Hz ac would be 50.6 μm at 300°K or 23.8 μm at 77°K, which is the more serious limitation. This means that if we both cool the copper to 77°K and allow $R_{MAX} = 25\ \Omega$, 32 layers of signal interconnects (49 total metal layers) are required to wire the maximal density 6" MCM, still an impractical large number for manufacturability. Using such a self-terminated line approach would probably require a certain number of different driver types, each having different source resistance characterisitics, therby complicating the design task.

As is pointed out in Section 3.1, plain $R_{MAX} = Z_O$, open circuit load/source terminated interconnections can tolerate somewhat over $R_{MAX} = 10\ \Omega$ line resistances without major degradation of the substantial CMOS noise margins. However, when the rather significant input capacitances which load the lines is considered, pulse edges with source termination are degraded relative to load termination, and that is made even worse when higher resistance, self-terminated

lines are used. Consider, for example, a 10pF board capacitance on an $R_L = 50\ \Omega$ terminated line, which will have a 550 ps rise time, but with a $Z_O = 50\ \Omega$ source-terminated line, the rise time is 1.1 ns. Hence, while source termination is convenient and low power, it has high speed performance limitations relative to load termination which are only further aggravated as self-termination is approached.

A final potential method of reducing the number of copper layers required to wire large maximal density MCMs is to relieve the constraint that all lines have the same width. In IC design, it is common to use narrower (higher Ω /cm) lines for the (numerous) shorter lines, and the wider line widths only for the longer lines. Unfortunately, in a MCM, simply increasing the line width alone doesn't help at all, since it correspondingly reduces the line impedance, Z_O, which makes the line proportionately more sensitive to R_{MAX}. However, if the dielectric layer thickness is increased in the same proportion, the line impedance will be preserved and the desired relative line ohmic resistance improved. Hence, it would be possible in an MCM to create two or more classes of signal interconnects, with wide copper traces and thick dielectrics for long lines and (higher density) narrower traces with thinner dielectrics for short lines. While this would require some substantial innovations in order for the CAD tools (particularly MCM routers) to support such an interconnect hierarchy (and routing software is already a serious problem for very complex boards), it is certainly theoretically possible to implement such an approach. While its practicability might be in question, the fact that there are so many short wires on a MCM makes it of interest. As opposed to the maximum signal line length of L_{MAX} = 12" on a 6" MCM, as discussed in Section 3.1 in conjunction with the Donath statistical wire length model, the average wire length for the same case is only ($\bar{R}$ = 4.6 for $N_R = 24$) $\bar{L}$ = 2.92 cm (1.15"). Hence, for 10^9 Hz and $R_{MAX} = 10\Omega$, a 77°K copper line width of 5.7 μm would be adequate for half of the interconnect wires. In a very simplistic view, this would mean that half of the MCM wires could be disposed of in 8 layers of signal interconnects, which would make a substantial reduction in the total number of signal layers required. Unfortunately, it is not quite that simple. If one assumes that the series termination approach outline in the previous section is not employed, a wide variability in the line geometrics may be required. In general, vias and other layout features of a size adequate for thick dielectric layers

and large trace sizes are not very compatible with interconnects an order of magnitude smaller in feature sizes. A series termination approach would have some of the issues referred to in the previous section. Hence, real design rule limitations will play a major role in how effective such a hierarchial dielectric thickness/variable line width approach would be in reducing the number of 77°K copper signal interconnect layers required to wire large maximal density MCMs. A wild guess might be a 2x reduction over the details of the layout design rules for the MCM technology.

In summary, several new normal metal interconnect MCM technology extensions have been considered which, if developed and adopted, could potentially reduce significantly the number of copper interconnect layers required to wire large, maximal density MCMs. If all of these (cooling to 77°K, using high resistance [self-terminated] interconnect lines, and routing in a hierarchy of dielectric layer thicknesses and line widths according to signal line length) were used at the same time, and if the rise times of the logic signal pulses were fairly slow, then it might even be possible to reduce the number of copper interconnect planes to something such might be manufacturable (given the existence of very effective in -process inspection and repair capabilities, and, of course, assuming that the very large stress levels that build up in organic dielectric MCM systems at cryogenic temperatures don't give insurmountable reliability problems).

However, if this can all be done in a simple, two signal layer HTSC MCM, which will work with today CAD tools (routers, etc.), which will work with any kind of signal interconnect termination scheme (eg., source or load terminated), and which will work with even the fastest of today's integrated circuit technologies, and indeed with the fastest expected in the foreseeable future, and do all of this without the performance and design compromises discussed above, and further yet be potentially cheaper, in the long term why would anyone want to consider anything short of the HTSC MCM technology? The issue is not whether HTSC MCMs are worth doing, it is whether we can in fact master the technology to build them. The prospects look good; it is time to go for it.

1.2. Program Directions

When we first began this HTSC-MCM study at Quad, nearly all discussion in the published literature had suggested that superconducting interconnects do not add any measurable benefit to high performance electronic systems. Since this project began we in essence had to work against a negative environment which all in all really proved helpful in forcing us, going in, to address issues that we may have had to put off for later times.

Many people in the past had looked at supercomputers operating at 77°K due not only to the benefit accrued from the decrease of the impedance of copper wires at these low temperatures, but also due to the factor of 3 to 4 increase of the speed of CMOS chips at the same temperatures. So there were incentives over a decade ago to operate at low temperatures and indeed much studies and real work was already accomplished in this area. At the same time much work was done by Quad and its consultants in the field of MCM technologies. Here it was recognized that the electronics industry is undergoing yet another revolution in high density integration using conventional semiconductor processing operating at room temperature. This conventional MCM technology, while it promised significant improvement at the module and system level, had met severe limitation for MCM as was experienced by IBM. This company reverted to complicated processes in order to manufacture MCMs having greater than 30 metallization layers. Our preliminary work had suggested that with HTSC-MCM only two signal layers would accomplish the same feat thereby significantly simplifying the MCM manufacturing process and perhaps culminating in higher performance, higher reliability, and lower cost system. So indeed we had a strong incentive to push for this technology. The problem however of translating the concept from a paper study to a working process that would execute and develop this technology was not as easy as it seemed. Many issues were before us (a) to convince the HTSC community of the potential benefit of HTSC-MCM (b) to convince system houses of the system benefits born out of this technology (c) since only few merchant HTSC vendors were available to work with, and since these vendors had virtually no MCM background, the question was how to bring to them MCM know-how in technology, marketing and manufacturing (d) to

ensure that whatever knowledge had been gained from people who worked a decade ago on low temperature supercomputer, that some how it be added to this project (e) and finally, if this technology is to benefit both commercial and military systems, that this project from the outset should include commercial and military players and should leverage on resources and assets from both sides of the industry sectors.

Our task, which initially began to study the market of systems using HTSC-MCM's, was sidetracked a bit in order to help put together a team that would address the issues raised in points (a) through (e). It was clear from earlier work that elements of an MCM infrastructure were as shown in Fig. 1-3a. We needed merchant foundries, we needed CAE Tools, we needed testing, we needed CAD applications, we needed cooling technologies and eventually we will need CMOS operating at Cryogenic temperatures.

Our efforts led to the formation of a team structure as shown in Fig. 1-3b. Here as can be seen we have all the elements needed to do the job.

The central role is played by the foundries. These are the players who have to solve the most difficult material and MCM manufacturing processes. Towards this end the team was structured so that all materials and processing research wherever performed would transition to the foundries. n-chip was added to educate these foundries on MCM manufacturing. Datamax, a spin-off from ETA, added the low temperature experience gained from the development of the ETA-10. Cray was also added to monitor the development of this technology and help guide it to commercial applications. E-Systems with its extensive MCM application know-how was a natural to lead the project and guide the technology for military application. Now the team is in place; the contract was awarded to E-Systems. A kick-off of the program is scheduled for October 24, 1991.

The other aspect of the effort at Quad was spent on the potential market of HTSC-MCM and MCM applications. These are discussed in the fourth quarter report. In effect our work shows that HTSC-MCM technology, particularly when

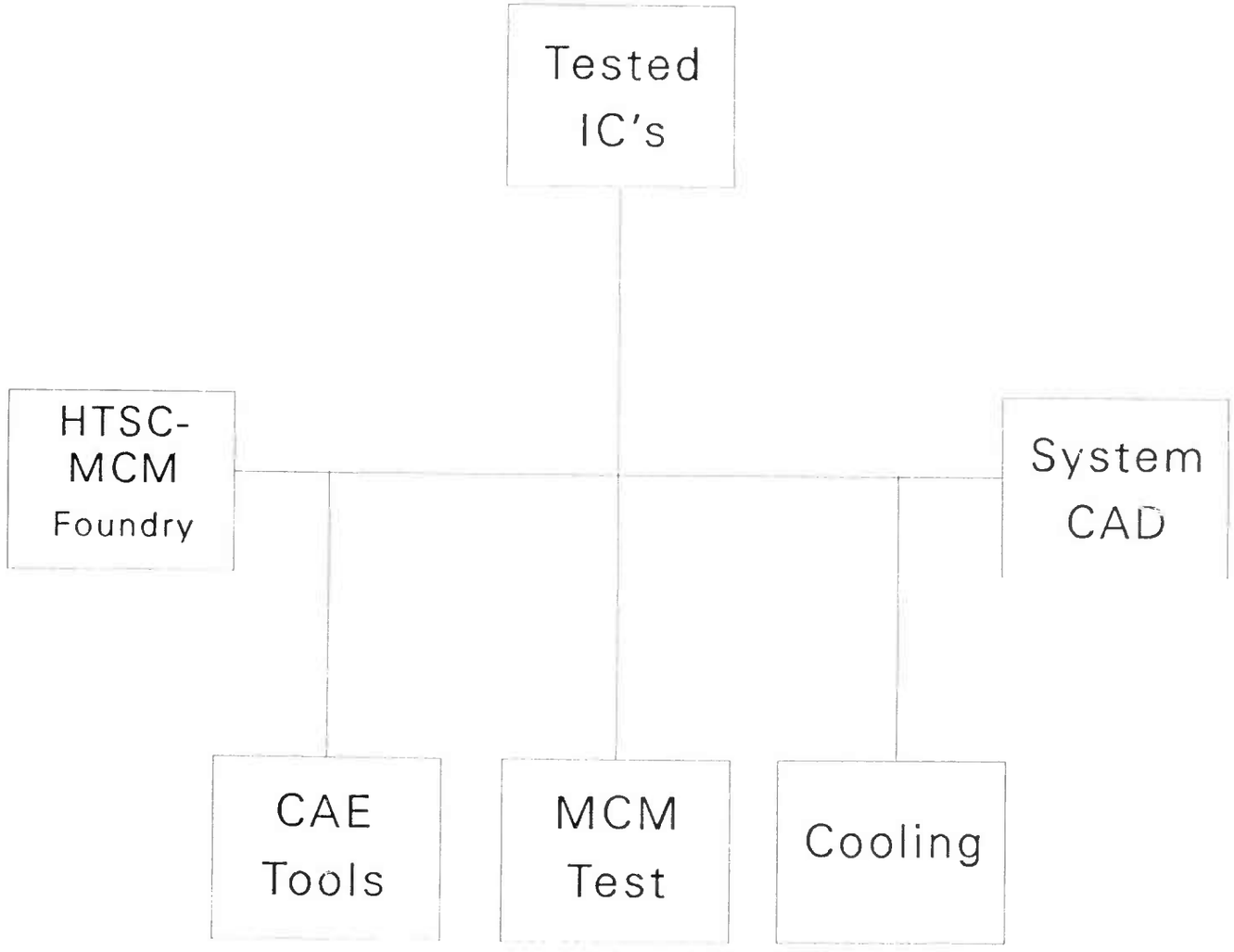

Tested
IC's
HTSC-
MCM
Foundry
System
CAD
CAE
Tools
MCM
Test
Cooling

Figure 1-3a

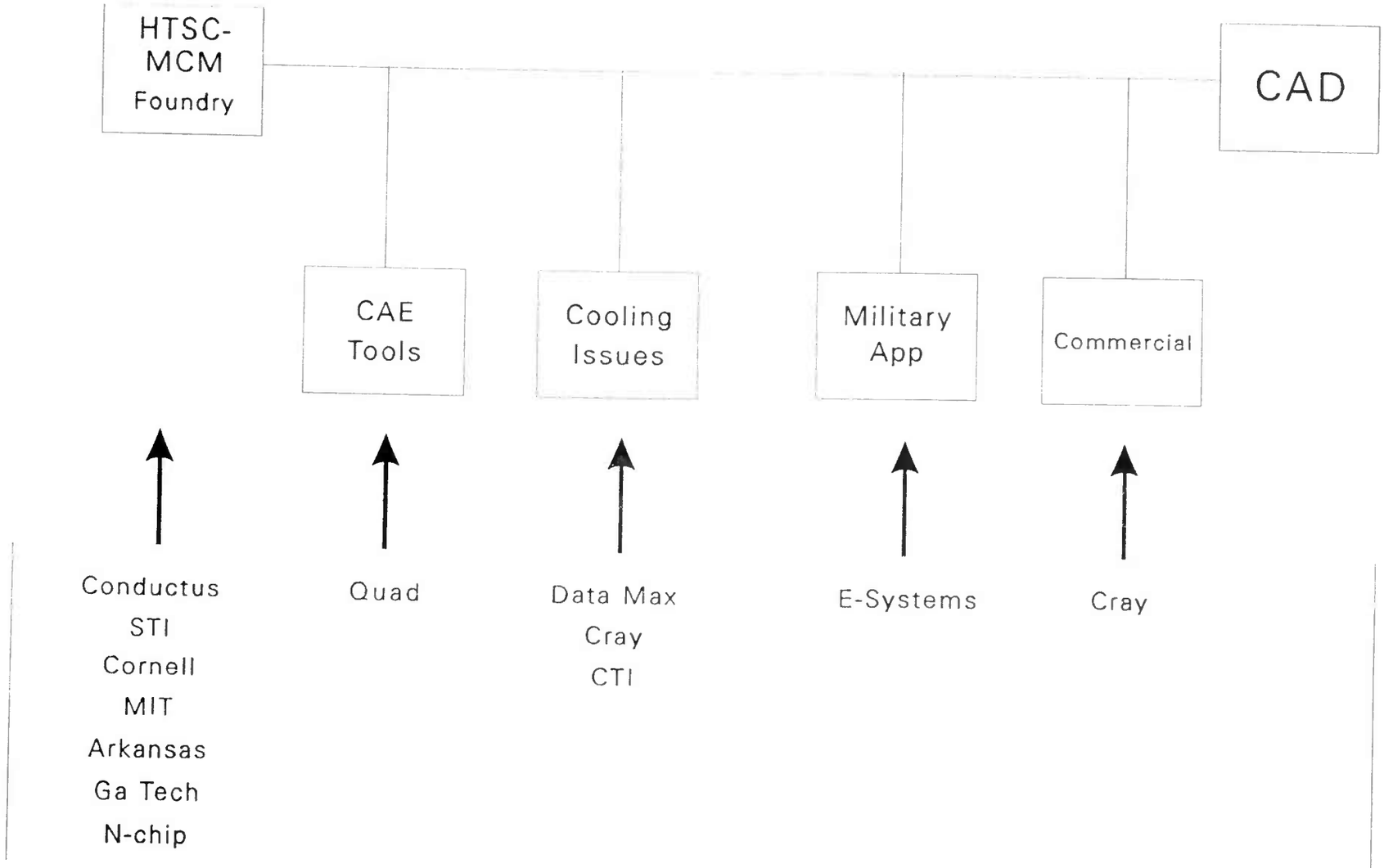

HTSC-
MCM
Foundry
CAD
CAE
Tools
Cooling
Issues
Military
App
Commercial
Conductus
STI
Cornell
MIT
Arkansas
Ga Tech
N-chip
Quad
Data Max
Cray
CTI
E-Systems
Cray

Figure 1-3b

combined with massively parallel process architecture, can have significant impact on applications ranging from minisuper computers to mainframes and supercomputers classes for both commercial and military applications. These applications could start benefiting from HTSC-MCM by the latter part of this decade and begin to serve as a stable market base for the HTSC - technology, with potential sales exceeding one billion dollars for bare HTSC-MCM's by the end of this decade or early 2000's.

Over the next two years however some key milestones need to be met, (a) demonstrate experimental validation of predicted HTSC-MCM benefits; (b) demonstrate concept feasibility of a low cost HTSC-MCM manufacturing process and (c) put in place the needed elements to have a viable merchant source which includes a complete merchant infrastructure and a market place, both commercial and military, read to insert and market the technology, and convince the semiconductor industry to lead an intensive effort in optimizing the CMOS technology for Cryogenic operations and help develop other salient technologies (CAE tools, testing, packaging) to make this highly promsing Cryoelectronics industry pay off to the commercial and military sectors.

SECTION 2

Q3 1991
QUARTERLY REPORT

Q3 1991 Quarterly Report

2.1. HTSC MCM Technology

As is noted in Section 3.3, concern was expressed (initially, in my awareness, by Prof. Ted VanDuzer of UC Berkeley) that the operating temperatures of the liquid nitrogen immersed IC chips might be so large as to preclude the use of YBCO as an HTSC MCM interconnect material. It is demonstrated in Section 3.1, using a nonlinear one-dimensional thermal model, that for the case of normal (face-up, wirebonded IC chips) die attached to the HTSC MCM substrate with low thermal conductivity (no silver, gold or diamond filling) epoxy material (or better yet, as suggested by the Livermore people, epoxy filled with the vacuum microspheres that are available), 90% or more of the heat can be made to go directly into the liquid nitrogen, and the temperature rise (above 77°K) at the HTSC substrate can be kept to about 3°K, even for a 10W/cm^2 power density, where the IC chip temperature rise would be 9.3°K.

A substantial level of effort in this program has been expended in describing the HTSC MCM concept and the work done on it, (as well as the future plans and applications interests for the program) to various individuals or groups in order to elicit their response. In particular, potential problems that are brought up are carefully noted for further investigation where appropriate, in order to assure that no "show stoppers" have been overlooked in the HTSC MCM concept. (None have been identified to this point, I might hasten to add.) The work on the magnetic field strengths around narrow lines and the die/HTSC interconnect temperature modeling just described are examples of efforts initiated because of concerns expressed by knowledgeable scientists in the HTSC field contacted through seminars, papers presented at workshops, etc.

In recent presentations on the HTSC MCM, including those at the Fallen Leaf Lake Workshop on Superconducting Electronics and the DARPA HTSC Conference in Seattle, our recent thermal modeling work described above was presented. This has

been generally quite favorable received, but with some specific helpful concerns expressed. One of these is the issue of flip-chip bonding of the die in order to reduce bonding cost and maximize the chip I/O count and minimize wasted "real estate" on the MCMs. The presence of large numbers of solder bumps joining the die and the HTSC interconnects, could, as noted in the Q2 1991 report, bring the HTSC temperature much closer to the IC die temperature than for the epoxy die attach case. These appear to be solutions for this case as well. We will treat this flip-chip case in later extensions to this work

Another concern, mentioned by Ted Van Duzer and several others, is that even in the epoxy die attached "normal" mounting case, the heat flow through the bond wires might bring the spot temperature at the wire to substrate bond point too high for the use of YBCO-type HTSC materials ("Thallium" would of course still be ok). The thermal conductivity of gold increases from 318 W/m °K at 300°K to 352 W/m °K at 77°K, while aluminium even more dramatically increases from 237 W/m °K at 300°K to 400 W/m °K at 80°K (the same as room temperature copper). While such high thermal conductivities might very well lead one to view the bond wires as a "thermal short" down to the substrate, I have pointed out in these various conversations that the bond wires are very fine (with typical diameters of 0.75 mils [0.019 mm] or 1.0 mils [0.025 mm]) and fairly long (of the order of 60 mils [1.5 mm] for the thick epoxy die attach layers considered here). Because of the high heat transfer coefficient from the wire to the liquid nitrogen due to nucleate boiling, the temperature in the wire may quite quickly approach the 77°K liquid nitrogen saturation temperature. Since this is clearly not obvious to many intelligent people, it is worth a quantitative examination.

Fig. 2-1 shows the physical model and its electrical equivalent used to solve, for the linear case, the heat flow equations to give the temperature variation along the bond wire immersed in liquid nitrogen. The heat flow incident into the left side of the (tiny) "rod" is conducted along the length of the rod by the thermal conductivity, k(W/cm °K) of the metal (the R_M term in ther electrical equivalent), or lost to the liquid nitrogen due to the large nucleate boiling heat transfer coefficient, h (W/cm^2

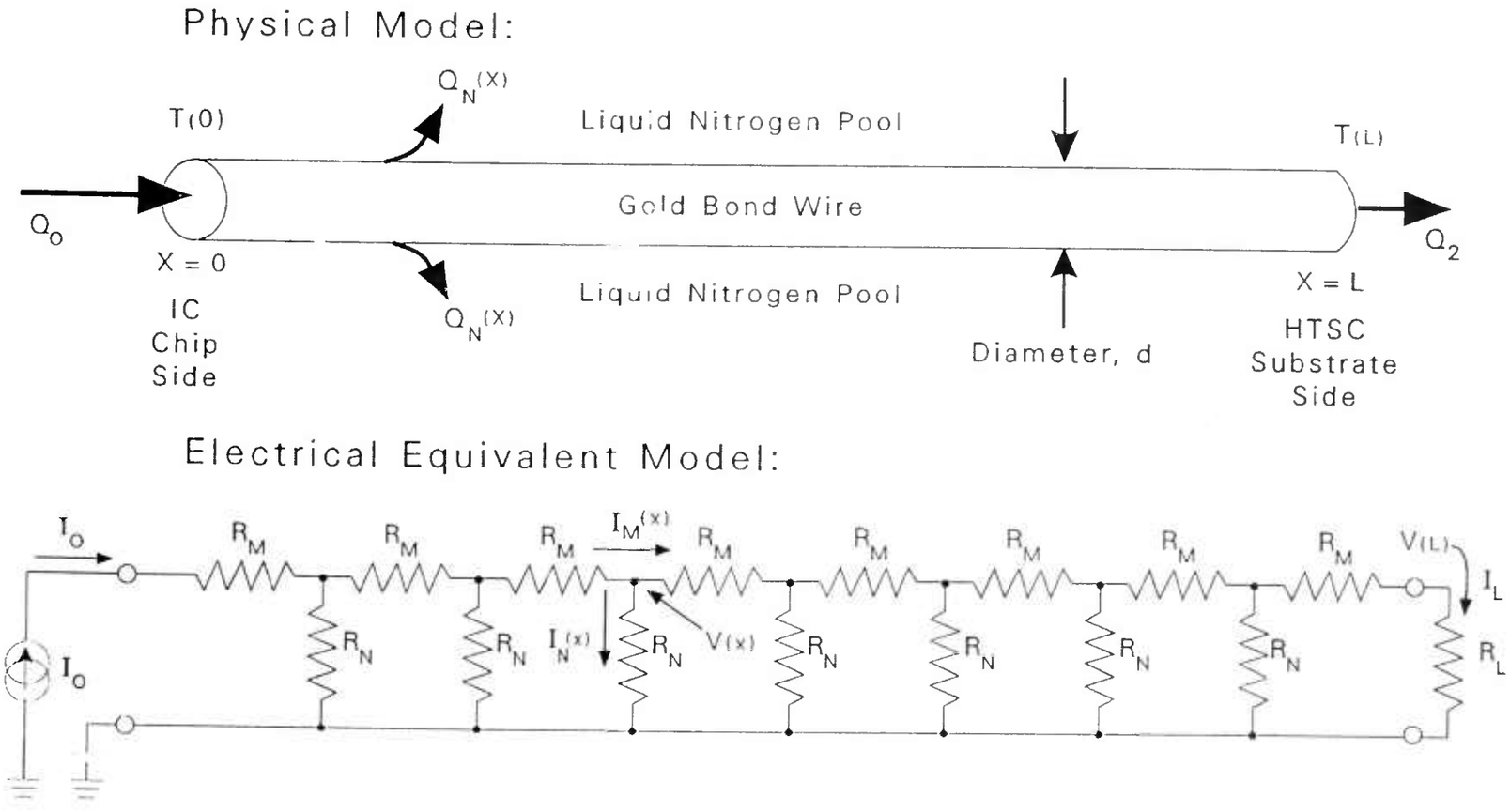

Physical Model:
$Q_N^{(X)}$
T(0)
Liquid Nitrogen Pool
T(L)
Gold Bond Wire
Q_o
Q_2
X = 0
Liquid Nitrogen Pool
X = L
$Q_N^{(X)}$
IC
Chip
Side
Diameter, d
HTSC
Substrate
Side
Electrical Equivalent Model:
I_o
R_M
$I_M^{(x)}$
V(L)
I_L
R_N
$I_N^{(x)}$
V(x)
R_L

Figure 2-1

°K), which gives rise to the R_N shunt term. Obviously, from the basic thermal resistance expression for thermal conduction,

$$R_{th} = \frac{L}{A\,k} \qquad \text{Eq.1}$$

the distributed wire thermal resistance per cm will be given by

$$R_M / L = \frac{1}{k\,A} = \frac{4}{\pi\,d^2\,k} \qquad \text{Eq.2}$$

where d is the bond wire diameter. The shunt conductance per unit length (here used as its reciprocal, the resistance-length product, $R_N L$), is given from the heat transfer coefficient, h, as

$$R_N L = \frac{L}{h\,A} = \frac{1}{\pi\,d\,h} \qquad \text{Eq.3}$$

where the entire peripheral area of the rod contacting the liquid is taken for A. As noted previously in conjunction with the liquid nitrogen pool boiling curve, the nucleate boiling power density (P/A) versus temperature rise above T_{SAT} = 77°K, ΔT, curve may be approximated in the region below ΔT = 10°K or so by

$$(P/A) = 0.0749\,\Delta T^{2.156} \qquad \text{Eq.4}$$

for (P/A) in W/cm^2. The "dc" heat transfer coefficient is given by

$$h = (P/A)/\Delta T \qquad \text{Eq. 5}$$

because the heat flow relationship in Eq.4 is not linear (2.156 is a long way from 1.000), the heat transfer coefficient, h, varies significantly with (P/A) or ΔT, and hence R_N varies as well. This means that the linear heat flow equations solved analytically here apply accurately over only limited sections of the wirebond in which the temperature change is not too large. At some later point in the program we will do a nonlinear numerical solution to get an accurate T(x) distrubution on the wirebonds, but the linearized solutions are quite adequate to give the insight we are looking for here (and we can break the wirebond into a number of shorter sections of nearby constant ΔT and integrate to obtain a numerical solution for any given case).

Table 2-1 shows the variation of h with ΔT for temperature rises of 1, 2, 3, 5, 7, and 10°K of the bondwire above the 77°K liquid nitrogen saturation temperature as caculated form Eqs. 4 and 5. This data is used to calculate the R_M and R_N values in Fig. 2-1 at each ΔT for the cases of d = 0.75 mil and d = 1 mil diameter of both gold and aluminum bond wires. Note that while h is quite good (over 1 W/cm^2 °K) at ΔT = 10°K, it drops off as $\Delta T^{1.156}$ power for lower temperature rises. For the most part, ΔT values below about 3°K are of for YBCO, so we need to consider heat transfer coefficients down to the 0.25 to 0.3 W/cm^2 °K range.

Consideration in Fig. 2-1 of the basic conduction equations gives for longitudinal conduction

$$I_M(x) = \frac{-1}{(R_M / L)} \quad \frac{dV(x)}{dx} \qquad \text{Eq. 5}$$

and for the transverse loss (I_N loss),

$$\frac{dI_M}{dx} = \frac{-V(x)}{R_N L} \qquad \text{Eq. 6}$$

Temperature Distribution on Gold And Aluminum Bond Wires in Liquid Nitrogen

Temperature Distribution along Bond Wire Immersed in Liquid Nitrogen

k (Gold)= 3.52 | k(Aluminum)= 4 | π = 3.1416 | 1 mil in cm= 0.00254 | Kt= 0.0749 | Nt= 2.156 | P/A=Kt*ΔT^Nt For Nucleate Pool Boiling "dc" 0.0749116

Wire Material	T=80°K k(W/cm °K)	Wire Dia. d (mils)	Wire d (cm)	Rm/L(°K/Wcm)	ΔT (°K)	P/A(W/cm^2)	h(W/cm^°K)	Rn*L(cm°K/W)	Rz (°K/W)	Le (mm)	1.5 exp(-L/Le)=	Wire Diameter d (mils)
Gold	3.52	0.75	0.001905	99672.99	10	10.7287487	1.07287487	155.7421172	3939.96	0.3952886	2.25%	0.75
Gold	3.52	0.75	0.001905	99672.99	7	4.97256475	0.71036639	235.2191845	4842.00	0.4857889	4.56%	0.75
Gold	3.52	0.75	0.001905	99672.99	5	2.40728995	0.48145799	347.0537562	5881.49	0.5900783	7.87%	0.75
Gold	3.52	0.75	0.001905	99672.99	3	0.80024413	0.26674804	626.4031079	7901.61	0.7927536	15.07%	0.75
Gold	3.52	0.75	0.001905	99672.99	2	0.33386412	0.16693206	1000.95695	9988.41	1.0021182	22.38%	0.75
Gold	3.52	0.75	0.001905	99672.99	1	0.0749116	0.0749116	2230.519756	14910.49	1.4959404	36.69%	0.75
Gold	3.52	1	0.00254	56066.06	10	10.7287487	1.07287487	116.8065879	2559.08	0.45644	3.74%	1
Gold	3.52	1	0.00254	56066.06	7	4.97256475	0.71036639	176.4143884	3144.97	0.5609407	6.90%	1
Gold	3.52	1	0.00254	56066.06	5	2.40728995	0.48145799	260.2903172	3820.14	0.6813637	11.06%	1
Gold	3.52	1	0.00254	56066.06	3	0.80024413	0.26674804	469.8023309	5132.25	0.915393	19.42%	1
Gold	3.52	1	0.00254	56066.06	2	0.33386412	0.16693206	750.7177123	6487.66	1.1571464	27.35%	1
Gold	3.52	1	0.00254	56066.06	1	0.0749116	0.0749116	1672.889817	9684.64	1.7273632	41.96%	1
Aluminum	4.00	0.75	0.001905	87712.23	10	10.7287487	1.07287487	155.7421172	3696.01	0.4213791	2.84%	0.75
Aluminum	4.00	0.75	0.001905	87712.23	7	4.97256475	0.71036639	235.2191845	4542.20	0.5178527	5.52%	0.75
Aluminum	4.00	0.75	0.001905	87712.23	5	2.40728995	0.48145799	347.0537562	5517.32	0.6290256	9.21%	0.75
Aluminum	4.00	0.75	0.001905	87712.23	3	0.80024413	0.26674804	626.4031079	7412.37	0.8450781	16.95%	0.75
Aluminum	4.00	0.75	0.001905	87712.23	2	0.33386412	0.16693206	1000.95695	9369.96	1.0682616	24.56%	0.75
Aluminum	4.00	0.75	0.001905	87712.23	1	0.0749116	0.0749116	2230.519756	13987.28	1.5946778	39.04%	0.75
Aluminum	4.00	1	0.00254	49338.13	10	10.7287487	1.07287487	116.8065879	2400.63	0.4865666	4.58%	1
Aluminum	4.00	1	0.00254	49338.13	7	4.97256475	0.71036639	176.4143884	2950.25	0.5979648	8.14%	1
Aluminum	4.00	1	0.00254	49338.13	5	2.40728995	0.48145799	260.2903172	3583.61	0.7263361	12.68%	1
Aluminum	4.00	1	0.00254	49338.13	3	0.80024413	0.26674804	469.8023309	4814.47	0.9758122	21.50%	1
Aluminum	4.00	1	0.00254	49338.13	2	0.33386412	0.16693206	750.7177123	6085.97	1.2335222	29.64%	1
Aluminum	4.00	1	0.00254	49338.13	1	0.0749116	0.0749116	1672.889817	9085.00	1.8413753	44.28%	1
	k 80°K Thermal Conductivity				ΔT= T-77°K Temperature Rise		h Heat Transfer Coefficient to LN2		Rz Thermal "Impedance" of Wire in LN2	Le Thermal Attenuation Length(mm)	1.5 mm Line Temperature Attenuation	

R. C. Eden For Typical Bond Wire Length of L=1.5 mm

Table 2-1

Differentiating Eq. 5 and substituting in Eq. 6 for dI_m/dx gives Laplace's equation:

$$\frac{d^2 V(x)}{dx^2} = \frac{(R_M / L)}{(R_N L)} V(x) \qquad \text{Eq. 6}$$

The voltage (temperature) distributions solving this equation are of the form

$$V(x) = a e^{-\alpha x} + b e^{+\alpha x} \qquad \text{Eq. 7}$$

That this is the correct solution is noted by simply differentiating twice, giving

$$\frac{dV}{dx} = \alpha a e^{-\alpha x} + \alpha b e^{+\alpha x} \qquad \text{Eq. 8}$$

and

$$\frac{d^2 V}{dx^2} = \alpha^2 a e^{-\alpha x} + \alpha^2 b e^{-\alpha x} = \alpha^2 V(x) \qquad \text{Eq. 9}$$

which solves Eq. 6 as long as we take the temperature attenuation coefficient, α, as

$$\alpha = \sqrt{\frac{R_M / L}{R_N L}} \qquad \text{Eq. 10}$$

The reciprocal of α is an effective or charecteristic length over which temperature deviations from T_{SAT} = 77°K tend to expoenentially die out,

$$L_e = \frac{1}{\alpha} = \sqrt{\frac{R_N L}{R_M / L}} \qquad \text{Eq. 11}$$

There is also a "characteristic thermal impedance" for the wire immersed in liquid nitrogen. It is the thermal resistance seen looking into the end of a very long ($L >> L_e$) wire, the other end of which need not be connected to anything. This "thermal impedance", R_Z (°K/W), is found from (b = 0 in Eq. 7).

$$R_Z = \left.\frac{V(O)}{I(O)}\right|_{L=\infty} = \sqrt{(R_M / L)\ (R_N L)} \qquad \text{Eq. 12}$$

For the case of long lines ($L > L_e$), or lines terminated with a thermal resistance R_L close to R_Z, then the temperature disturbs die out exponentially with distance,

$$T(x) = T(o)\, e^{-x/L_e} \qquad \text{Eq. 13}$$

with the characteristic length, L_e.

In Table 2-1, values for this characteristic length, L_e, and for the "thermal impedance", R_Z, are shown for each case. For example, for a 0.75 mil gold bond wire we have $L_e = 0.395$ mm at $\Delta T = 10°K$, increasing (because of the lower h) to about twice that, $L_e = 0.792$ mm, at $\Delta T = 3°K$, with corresponding R_Z values of 3940 °K/W at 10°K and 7902 °K/W at $\Delta T = 3°K$. This means (doing a rough integral to handle the nonlinearity), and shown in the $\Delta T = T - 77°K$ versus distance along bond wire plot in Fig. 2-2, that if we have a chip temperature of $\Delta T = 10°K$ at one end of a 0.75 mil gold thermally matched terminated bond wire, the ΔT at a distance of 0.5 mm (19.7 mils) down the wire, the temperature rise will be only 3.9°K and 1.0 mm (39.37 mils) down the wire the temperature rise will be only 2.1°K. For a typical 1.5 mm (59 mils) bond wire length, at the HTSC substrate end, the ΔT will be only 1.32° above the 77°K liquid nitrogen saturation temperature. Hence, standard 0.75 mil gold bond wires do not represent a "thermal short" in normal lengths. As seen in Table 2-1, larger diameter wires will cause greater temperature rises, and aluminum is slightly worse than gold.

2.2. MCM Technology Applications

The superconducting MCM (SC-MCM) technology applications clearly seem to be destined to span from supercomputer class to certainly mini supercomputer class applications. For the superconducting vendors selling SC-MCM could render significant stability to their operations. During the last three months we have tried to bring together several elements of the infrastructure to ensure that as this technology is developed, at least some specter of the market can start to develop right along with it. The idea being that once the technology has matured, maybe the market would be there for it; even though the market and the technology are not expected to mature until 1995, it is still prudent that they grow up simultaneously. Towards this goal we have tried to ensure that the team includes all the necessary features such as foundry CAE Tools, system design, refrigerative or cooling packaging, etc. In particular the main focus was on real MCM foundry and MCM applications. Currently the team has no MCM capabilities, meaning that STI and

Temperature vs. Distance Along 0.75 mil (0.019 mm) Diameter Gold Bond Wire Immersed in Liquid Nitrogen for ΔT(chip)=10°K

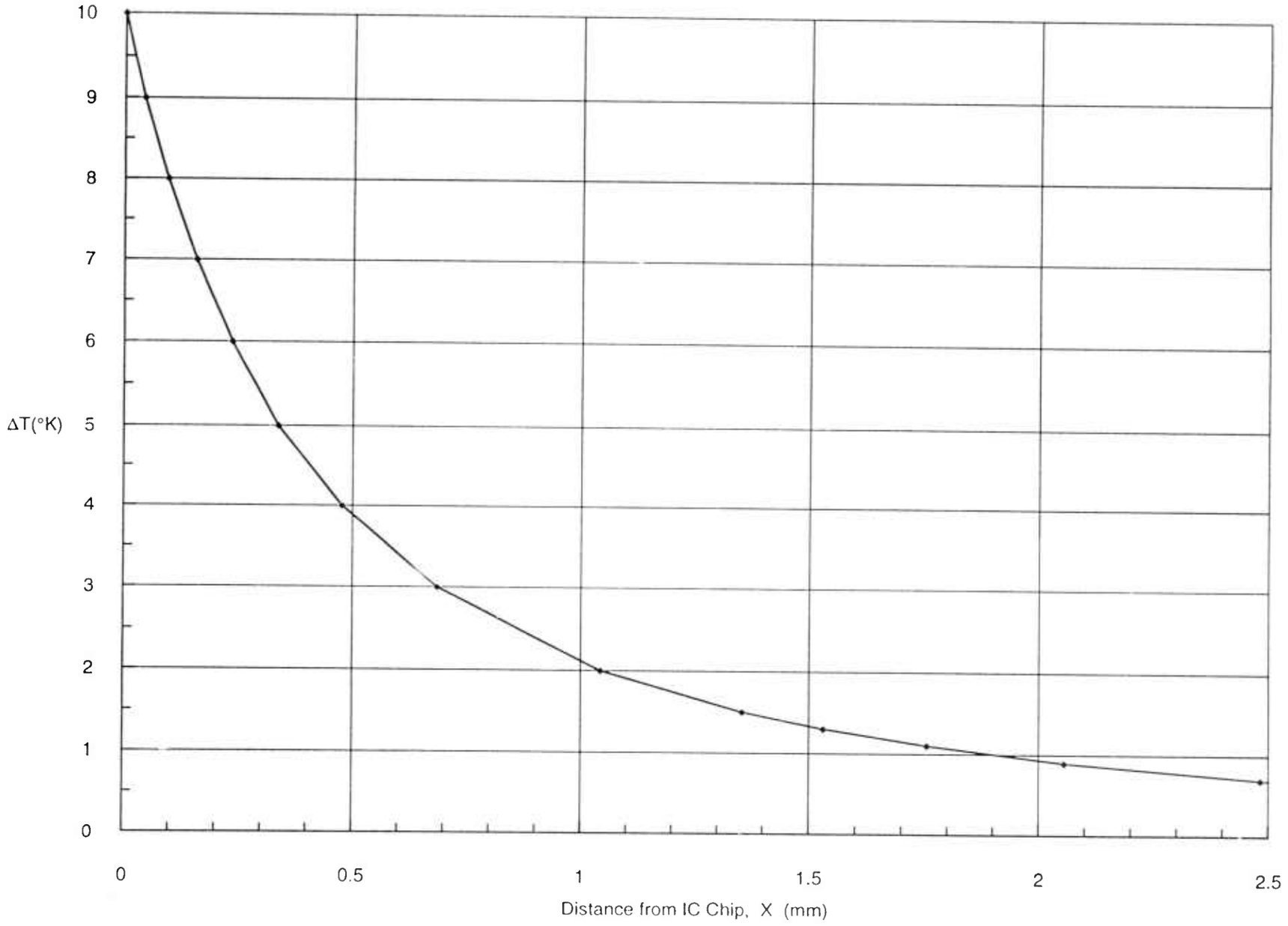


Figure 2-2

conductus do not have any background in MCM technology development, or digital semiconductor manufacturing know-how. For that reason, we have tried and have succeeded in convincing N-chip to play a role on our team in order to add such expertise and know-how to the team. Towards this end, n-Chip has agreed to provide facility and MCM capacity so that superconductivity engineers and scientist can visit, have a place to stay, work, and use n-Chip people and equipment to learn MCM technology and manufacturing know-how. Further, the n-Chip engineers have already interacted on the SC-MCM fabrication process even prior to the invitation of the programmer, and provided already made significant input that could assist the growth of the SC-MCM technology.

In a different area, we began serious discussions with Tony Vacca at Cray regarding the identification of a machine that could use SC-MCM within four years. Dr. Vacca recommended the Cray E-L machine which is equivalent to a mini-supercomputer. This has a large PC board containing over 30 interconnect layers and probably 200 CMOS chips. This board could be converted to a SC-MCM with only a process control role in MCM development and solution. Also upon request from several congressional staffs, a detailed presentation was prepared and given on SC-MCM to the house and senate authorization committee staff.

2.3. HTSC MCM Applications

A number of Market research firms, we understand, have done market surveys for the MCM technology application. We have not had access to these reports. However, it seems obvious that no market projection can be so credible without fully taking account of the application needs and the various MCM technologies that will evolve during the next decade. It is our opinion that several major MCM technology thrusts will be developed this decade. These include conventional MCM, 3-dimensional MCM, superconducting MCM and advanced multi signal layer (>2) conventional MCM. In Table 2-2, we show the projections we made based on industry discussions. It seems to us that the conventional (2 signal layers) will dominate the low end from PC to the mini-supercomputer, 3-D will cover high end work station to the supercomputer while SC-MCM will cover mini-supercomputer through supercomputer. In special applications it is conceivable that SC-MCM will also play a role in embedded processors. In any case, the market that SC-MCM addresses should exceed one billion dollars, giving a good chance for merchant vendors to establish a stable source.

The issues that are critically upon us have to do with market penetration: How to facilitate the acceptance of this technology by commercial and military houses.

YEAR 2000

MILITARY PRODUCT SEGMENTS	COMM PRODUCT SEGMENTS	NUMBER OF SYSTEMS	NUMBER OF MCM/SYST.	NUMBER OF MCM	PRICE PER	MARKET $M	CONVENTIONAL MCM	3-D MCM	SUPER CONDUCTING MCM
HI PERF PROCESSOR	SUPER COMPUTER	400	46	20,000	2,000	2,000			
DATA PROCESSOR	MAIN FRAM	7,000	30	210,000	1,000	210			
SIGNAL PROCESSOR	MINI SUPER	100,000	20	2,000,000	750	1.5 B			
W/S GRAPH IMAGER	WORK STATION	5,000,000	4	20,000,000	200	4 B			
IAI	PALM SIZE	10,000,000	1	10,000,000	100	1 B			
LOW COST IMAGER	PC	20,000,000	2	40,000,000	100	4 B			
EMBEDDED (AVERAGE)	EMBEDDED	10,000,000	4	40,000,000	200	8 B			

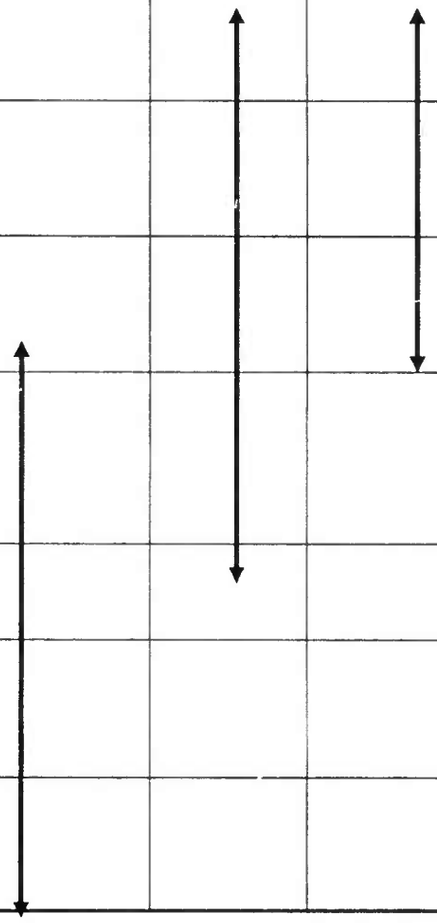


Table 2-2

2.4. Analytic Expressions for Frequency Dependent Transmission Line Parameters

This is a summary of work performed under this contract by Professors Antonije Djordjevic & Tapan Sarkar of the Syracuse University in the area of resistive and inductive transmission line models for normal microstrip & stripline lines.

For microstrip, the propagation of quasi-TEM waves can be analyzed in two ways. The first one is the pure field-theory approach, which essentially start from Maxwell's equation. The solution yields the structure of the electromagnetic field and the propagation coefficient of the wave.

The second approach is a combination of the field theory and the circuit theory. In this approach, the transmission line primary parameters, i.e., the inductance per unity length (L'), the capacitance per unit length (C'), the resistance per unit length (R') and the conductance per unit length (G'). are evaluated using the field theory. Thereby, the fields are assumed to be quasi-static (i.e., slowly varying in time), and

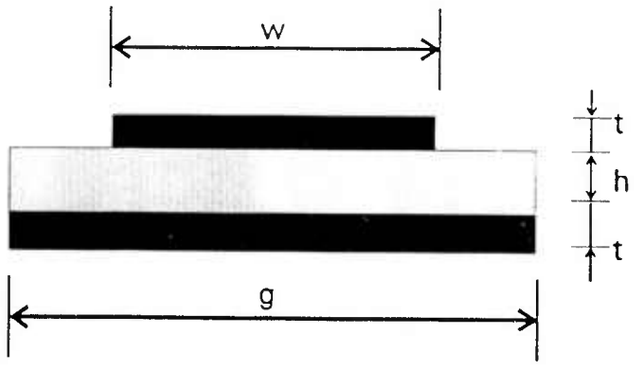


Figure 2-3: Cross Section of a Microstrip Transmission Line

the analysis is separated into two independent parts. In the first part, the electrostatic case is considered, involving only the electric field in the dielectric and the conductor charges, and the capacitance is evaluated. By taking the dielectric permittivity to be complex, from the electrostatic analysis the conductance is

evaluated, too. In the second part, the magnetic field is considered, together with the electric field in the conductors, resulting in the inductance and resistance. Once the transmission line primary parameters are known, the secondary parameters (the characteristic impedance and the propagation coefficient) are obtained form the circuit-theory approach.

Here, we will consider only the quasi-static analysis of the inductance and resistance. We suppose that the transmission line conductors carry equal steady-state currents, which are opposite in direction, of root-mean-square (rms) value I and frequency f.

At low frequencies (towards the d.c. end), the currents are uniformly distributed over each conductor cross section. As the frequency increases, due to the induced electric field, the current distribution starts changing. This effect is, for the purpose of a simpler explanation, separated into three parts (although everything is due only to the induced field). The first part is the edge effect, where the current tends to concentrate at the sharp edges of a conductor. This effect affects both the signal conductor and the ground conductor. However, it is more pronounced in the signal conductor, because in the ground conductor, the second effects usually dominates.

The second part is the proximity effect, where the presence of one conductor influences the current distribution in the other conductor. As a consequence, the current in the ground conductor tends to concentrate below the signal conductor (instead of being spread along the whole width of the ground conductor). Also, the edge effect in the signal conductor is somewhat smaller than if there were no ground conductor.

The third part is the skin effect, pronounced at high frequencies in both conductors, where the current becomes concentrated within layers at the conductor surfaces. The thickness of a layer is of the order of several skin depths δ, where the skin depths is defined by

$$\delta = \frac{1}{\sqrt{\pi \mu f \sigma}} \quad , \qquad \text{Eq. 1}$$

where $\mu = \mu r \mu o$ and $\mu o = 4\pi\ 10^{-7}$ Hm . A practical formula for copper (at room temperature) is

$$\delta Cu = \frac{67\ \mu m}{\sqrt{f}} \qquad \text{Eq. 2}$$

where the frequency is expressed in MHz.

Due to the variations of the current distribution, the transmission line inductance and resistance per unit length vary with frequency. Up to a certain frequency, at the low-frequency end, the inductance and resistance are practically constant. Thereafter, at medium frequencies, due to the concentration of the current (i.e., reduction of the effective conductor cross section) the resistance starts increasing. This concentration modifies the external inductance per unit length. Simultaneously, the magnetic field within conductors is reduced, resulting in a decay of the internal inductance, which contributes to the decay of the total inductance. The transition between the low-frequency and the medium-frequency regions is related to the ratio R'/L', as will be shown later.

At high frequencies, when the edge, proximity and skin effects are fully pronounced, the resistance per unit length increases as the square root of frequency. The inductance per unit length becomes practically constant, and it can be expressed as

$$L'_{\infty} = \frac{\varepsilon o \mu o}{C'_o} \qquad \text{Eq. 3}$$

where $\varepsilon = 8.8542 \cdot 10^{-12}$ F/m is the permittivity of vacuum, and C'_o is the transmission line capacitance per unit length when the dielectrics are substituted by vacuum. More precisely, the inductance per unit length has an additional small term which is inversely proportional to the square root of frequency, and which is due to the decrease of the internal inductance with the decrease of the skin depth. The transition between the medium-frequency and the high-frequency regions occurs when the conductor thickness becomes of the order of the skin depth.

Exact, analytical expression for the microstrip inductance and resistance per unit length, as a function of frequency, are not known. The analysis of such transmission lines can, however, be performed numerically, and there exist several published methods. For the present purpose, where the accuracy at the low-frequency end seems to be important, we have chosen a technique which we will refer to as the volume-current formulation.

Based on an interpolation of these results and on some theoretical considerations, a set of closed-form formulas has been derived.

At low frequencies, the current distribution is practically uniform within one conductor. However, at higher frequencies the current distribution starts changing, which results in variations of both the inductance (which starts decreasing) and resistance per unit length (which starts increasing). Here starts the medium-frequency range. As the frequency increases further, the proximity and edge effects become fully pronounced, and the skin-effect region starts. In this high-frequency region, the current is localized in a thin layer at the conductor surface. The depth of the layer decreases with frequency, according to equation (1), i.e., it is proportional to $1/\sqrt{f}$. However, the equivalent surface-current proportional to 1/f (for a constant excitation field). Hence, the resistance increases as $\sqrt{f}$, the external inductance of the line is practically independent of the frequency, and the internal inductance is proportional to $\sqrt{f}$. Mathematically, the resistance and inductance per unit length in the high-frequency region asymptotically behave as

$$R'(f) \rightarrow R'_S(f) = R'_S(f_i)\sqrt{f/f_i} \qquad \text{Eq. 4}$$

$$L'(f) \rightarrow L'_\infty + R'_S(f)/\omega \qquad \text{Eq. 5}$$

where $\omega = 2\pi f$, f_i is chosen (reference) frequency, $R'_S(f)$ denotes the skin-effect resistance. The low-frequency resistance per unit length (i.e., the d.c. resistance) of a microstrip line, having conductor width w, and ground plane width g and having metal thickness t.

$$R'(0) = R'_{go} + R'_{wo} \qquad \text{Eq. 6}$$

where

$$R'_{go} = \frac{1}{\sigma g t} \qquad \text{Eq. 7}$$

is the resistance per unit length of the ground conductor, and

$$R'_{wo} = \frac{1}{\sigma w t} \qquad \text{Eq. 8}$$

is the resistance per unity length of the signal conductor. Equations (7) and (8) follow from the calculation of the resistance of a flat-strip conductor.

The low-frequency inductance can be evaluated from energy considerations. The stored magnetic energy per unit length of the line can be expressed in terms of the inductance per unity length (L') and current (I) as

$$W'_m = \frac{1}{2} L' I^2 \qquad \text{Eq. 9}$$

Another calculation approach is possible by assuming the conductors to be very thin (i.e., $t < w,g$), so that the effects of the internal inductance are relatively small. In that case, the conductors with volume currents can be approximated by surface-current sheets, of surface-current densities $J_{S1} = I/w$ (signal conductor) and $J_{S2} = I/g$ (ground conductor). Following a similar approach as above, the inductance per unit length is given by

$$L_o' = L'(0) \approx -\frac{\mu o}{2\pi}\left\{\frac{1}{w}\int_{w/2}^{-w/2}\int_{w/2}^{-w/2}\log|(x-x')|dx'\,dx\right.$$

$$\frac{-2}{wg}\int_{-w/2}^{w/2}\int_{-g/2}^{g/2}\log\sqrt{(x-x')^2+(h+t)^2}\;dx'\,dx$$

$$\left.+\frac{1}{g^2}\int_{w/2}^{-w/2}\int_{w/2}^{-w/2}\log|(x-x')|dx'\,dx\right\} \qquad \text{Eq. 10}$$

where h + t is the separation between the conductor planes of symmetry. These integral can also be evaluated explicitly. The internal inductance of a thin strip conductor, of width w and thickness t, which is approximately included in the above equation, is given by

$$L_i' = \frac{\mu o}{12}\frac{t}{w} \qquad \text{Eq. 11}$$

For the high-frequency region, when the skin effect is fully developed, there exist approximated, closed-form formulas for the quasi-static transmission line parameters. One set of such formulas is given, for example, in Reference. From these formulas it is straightforward to obtain

$$L_\infty' = L'(\infty) = Z_{co\infty}/c_o \;, \qquad \text{Eq. 12}$$

$$C' = L_\infty'/Z_{C\infty}^2 \;, \qquad \text{Eq. 13}$$

where

$$c_o = \frac{1}{\sqrt{\varepsilon_o \mu_o}} \approx 3 \cdot 10^8 \text{ m/s} \quad , \qquad \text{Eq. 14}$$

is the velocity of light in vacuum, $Z_{C\infty}$ is the characteristic impedance of the microstrip line in the high-frequency region, and $Z_{Co\infty}$ is the characteristic impedance in the same frequency region when the dielectric is removed. These impedances are related by

$$Z_{C\infty} = C_{C\infty} / \sqrt{\varepsilon_{re}} \quad , \qquad \text{Eq. 15}$$

where ε_{re} is referred to as the effective relative permittivity of the line.

The approximate expression of the resistance per unit length in the high-frequency region is:

$$R' = \frac{R_S}{\pi h} \frac{32 - \left(\frac{w}{h}\right)^2}{32 + \left(\frac{w}{h}\right)^2} \left[1 + \frac{h}{w}\left(1 + \frac{\partial_{w_e}}{\partial t}\right)\right] \quad , \frac{w}{h} < 1 \quad ,$$

Eq. 16

$$R' = \frac{2}{h} \frac{\varepsilon_{re} Z_C^2 R_S}{Z_O^2} \left\{\frac{w}{h} + \frac{6h}{w}\left[(1 - \frac{h}{w})^5 + 0.08\right]\right\} \left[1 + \frac{h}{w}\left(1 + \frac{\partial_{w_e}}{\partial t}\right)\right] , \frac{w}{h} > 1 \quad ,$$

Eq. 17

where

$$\frac{\partial_{w_e}}{\partial t} = \frac{1}{\pi} \log \frac{2h}{t} \quad , \; w < h / 2\pi \quad , \qquad \text{Eq. 18}$$

$$\frac{\partial_{w_e}}{\partial t} = \frac{1}{\pi} \log \frac{4\pi w}{t} \quad , w > h/2\pi \quad , \qquad \text{Eq. 19}$$

and

$$R_s = \sqrt{\frac{\pi \mu f}{\sigma}} = \frac{1}{\sigma \delta} \quad , \qquad \text{Eq. 20}$$

is the surface resistance of the conductor.

Although the formulas for L' and R' at low and at high frequencies are available, as shown above, there are no known exact or approximate expressions for the values in the medium-frequency region. Extensive numerical experiments have shown that relative simple approximations for the variations of the inductance and resistance in this region seems to be sufficient of practical purposes. These formulas are presented below.

First we have to define the boundaries of the medium-frequency region. The lower boundary is the frequency at which the resistance and inductance start changing from their d.c. values, and the upper boundary is the frequency at which equation (5) becomes valid.

Extensive numerical experiments have shown that the upper boundary of the low-frequency region, i.e., the lower boundary of the medium-frequency region, is approximately given by

$$f_o = \frac{2}{\mu o} \frac{R'_{go} R'_{wo}}{R'_{go} + R'_{wo}} \quad , \qquad \text{Eq. 21}$$

where R'_{go} and R'_{wo} are given by equation (7) and (8), respectively.

The boundary between the medium-frequency and high-frequency regions is given by

$$f_S = \frac{1.6 + \frac{10\,t/w}{1 + w/h}}{\pi \mu \sigma t^2} \quad , \qquad \text{Eq. 22}$$

First, we evaluate $R'_\infty(f_\infty)$ from equations (1.36-37) at a frequency f_∞ which is assumed to be in the high-frequency region. (Actually, f_∞ = 1 Ghz in the program, but this frequency need not be greater than f_S.) Next, we evaluate the skin-effect region resistance extrapolated to f_S as

$$R'_S(f_S) = R'_\infty(f_\infty)\sqrt{\frac{f_S}{f_\infty}} \quad , \qquad \text{Eq. 23}$$

Now, tne resistance and inductance per unit length are given by

$$R'(f) = R'_O + \frac{R'_S(f_S)\,\frac{\sqrt{f/f_S} + \sqrt{1 + (f/f_S)^2}}{1 + \sqrt{(f/f_S)}} - \left[R'_S(f_S) - R'_O\right] F(f) - R'_O}{1 + \frac{0.2}{1 + w/h}\log(1 + f_S/f)} \quad ,$$

Eq. 24

$$L'(f) = \frac{R'_S(f_S)\,\sqrt{f/f_S}}{2\pi f\,(1 + \sqrt{f_S/f})} + L'_\infty + \left[L_O - L_\infty - \frac{R'_S(t_S)}{2\pi f_S}\right] F(f) \quad ,$$

Eq. 25

where

$$F(f) = \frac{1}{\sqrt{1 + \left(\frac{f}{f_o}\right)^2}}, \qquad \text{Eq. 26}$$

and $R'_o = R'(0)$.

Strip transmission lines (striplines) are much more frequent in fast digital circuits (transmission lines at all the inner layers of a printed-circuit board). The cross section of a stripline is shown in Fig. 2-4. The total dielectric thickness is (2h + t), its relative permittivity is ε_r and loss tangent tg δ . The thickness of the signal conductor and the ground conductors is t, their conductivity is σ, and relative permeability μ_r . The signal conductor width is w, and the ground conductor width is g (and it is assumed to be much larger than h, but finite).

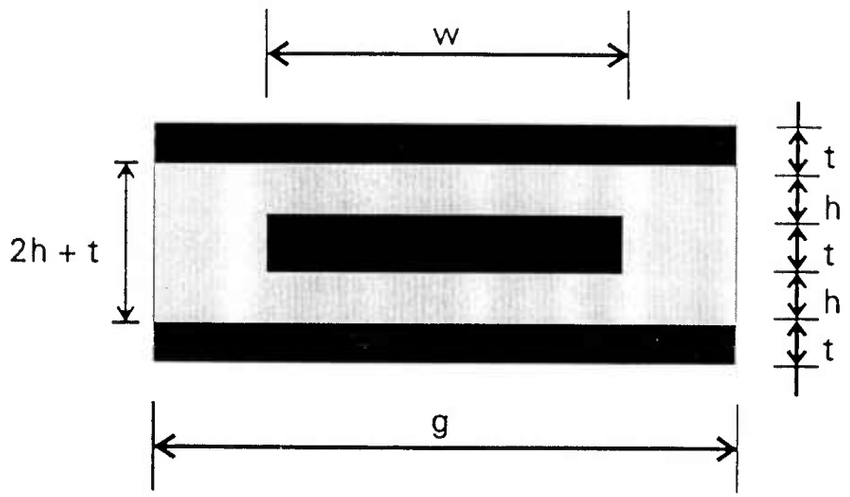


Figure 2-4: Cross Section of a Strip Transmission Line

Exact, analytical expression for the stripline inductance and resistance per unit length, as a function of frequency, are not known. The analysis of such transmission lines can, however, be performed numerically, for example, using methods similar to the previous section. Based on an interpolation of these results and on some theoretical considerations, a set of closed-form formulas has been derived.

The frequency behavior of inductance and resistance per unit length of striplines is very similar to the same dependence of microstrip lines. As described previously, the frequency is divided into three ranges: the low-frequency range (starting from the d.c.), the medium-frequency range, and the high-frequency range (skin-effect region).

As before, low-frequency resistance per unit length (i.e., the d.c. resistance) of the stripline, sketched in Fig. 2-3, is given by

$$R'(0) = R'_O = R'_{go} + R'_{wo} \quad , \qquad \text{Eq. 27}$$

where

$$R'_{go} = \frac{1}{2\sigma g t} \quad , \qquad \text{Eq. 28}$$

is the equivalent resistance per unit length of the ground conductors, and

$$R'_{wo} = \frac{1}{\sigma w t} \quad , \qquad \text{Eq. 29}$$

is the resistance per unit length of the signal conductor.

Simple formulas of the low-frequency inductance can be obtained by assuming the conductors to be very thin (i.e., $t << w,g$), as explained previously. In that case we have

$$L'_o = L'(0) \approx -\frac{\mu o}{2\pi}\left\{\frac{1}{w^2}\int_{-w/2}^{w/2}\int_{-w/2}^{w/2}\log|(x-x')|dx'\,dx\right.$$

$$-\frac{2}{wg}\int_{-w/2}^{w/2}\int_{-g/2}^{g/2}\log\sqrt{(x-x')^2+(h+t)^2}\,dx'\,dx$$

$$\left.\frac{1}{2g^2}\left[\int_{-g/2}^{g/2}\int_{-g/2}^{g/2}\log|(x-x')|dx'\,dx\right.\right.$$

$$\left.\left.+\int_{-g/2}^{g/2}\int_{-g/2}^{g/2}\log\sqrt{(x-x')^2+(2h+2t)^2}\,dx'\,dx\right]\right\}, \qquad \text{Eq. 30}$$

These integrals can again be evaluated explicitly.

As for microstrip, the stripline high-frequency inductance per unit length (L'_∞) and the capacitance per unit length (C') can be evaluated form the high-frequency characteristic impedance of the stripline ($Z_{C\infty}$) and the velocity of wave propagation in the dielectric.

In the literature there exist approximate, closed-from formulas for the high-frequency characteristic impedance and the resistance per unit length (R'_∞) of striplines. After corrections, the formulas read:

$$Z_{C\infty} = \frac{30\,\Omega}{\sqrt{\varepsilon_r}}\log\left\{1+\frac{4}{\pi}\frac{b-t}{w'}\left[\frac{8}{\pi}\frac{b-t}{w'}+\sqrt{\left(\frac{8}{\pi}\,b-t\right)^2+6.27}\right]\right\}, \qquad \text{Eq. 31}$$

$$\frac{w'}{b-t} = \frac{w}{b-t} + \frac{\Delta w}{b-t} \quad , \qquad \text{Eq. 32}$$

$$\frac{\Delta w}{b-t} = \frac{x}{\pi(1-x)} \left\{ 1 - \frac{1}{2} \log \left[\left(\frac{x}{2-x} \right)^2 = \left(\frac{0.0796x}{w/b = 1.1x} \right)^m \right] \right\} \quad , \qquad \text{Eq. 33}$$

$$m = 2\left(1 + \frac{2}{3}\frac{x}{1-x}\right)^{-1} \qquad \text{Eq. 34}$$

$$x = \frac{t}{b} \quad , \qquad \text{Eq. 35}$$

$$b + 2h + t \qquad \text{Eq. 36}$$

$$R'_{\infty} = -\ 0.00532\ R_S \sqrt{\varepsilon_r} \frac{\partial Z_C^{\infty}}{\partial w'} \left[1 + \frac{2w'}{b-t} - \frac{1}{\pi} \left(\frac{3x}{2-x} = \log \frac{x}{2-x} \right) \right] \quad . \qquad \text{Eq. 37}$$

$$\frac{\partial Z_{C\infty}}{\partial w'} = \frac{30\, e^{-A}}{w' \sqrt{\varepsilon_r}} \left[\frac{3.135}{Q} - \left(\frac{8}{\pi} \frac{b-t}{w'} \right)^2 (1+Q) \right] \quad . \qquad \text{Eq. 38}$$

$$A = \frac{Z_o \sqrt{\varepsilon_r}}{30\ \Omega} \quad , \qquad \text{Eq. 39}$$

$$Q = \sqrt{1 + 6.27\left(\frac{\pi}{8}\frac{w'}{b-t}\right)} \quad , \qquad \text{Eq. 40}$$

where

$$R_S = \frac{\sqrt{\pi\mu f}}{\sigma} \quad , \qquad \text{Eq. 41}$$

is the surface resistance of the conductors.

The upper boundary of the low-frequency region, i.e., the lower boundary of the medium-frequency region, is approximately given again by equation 21.

Numerical experiments of both microstrip lines and striplines have shown that good boundaries between the medium-frequency and high-frequency regions can be given by

$$f_S = \frac{2.4 + \frac{10\,t/w}{1 + w/h}}{\pi\mu\sigma t^2} \qquad \text{Eq. 42}$$

First, we evaluate $R'_\infty(f_\infty)$ from equation (19) at a frequency f_∞ which is assumed to be in the high-frequency region. (Actually, f_∞ = 1 Ghz in the program, but this frequency need not be greater than f_S as

$$R'_S(f_S) = R'_\infty(f_\infty)\sqrt{\frac{f_S}{f_\infty}} \quad , \qquad \text{Eq. 43}$$

Finally, the resistance and inductance per unit length are given by

$$R'(f) = R'_O + \frac{R'_S(f_S)\,\dfrac{\sqrt{f/f_S} + \sqrt{1 + (f/f_S)^2}}{1 + \sqrt{(f/f_S)}} - \left[R'_S(f_S) - R'_O\right] F(f) - R'_O}{1 + \dfrac{0.4}{1 + w/h}\log\,(1 + f_S/f)} \quad ,$$

Eq. 44

$$L'(f) = \frac{R'_S(f_S)\,\sqrt{f/f_S}}{2\pi f\,(1 + \sqrt{f_S/f})} + L'_\infty + \left[L'_O - L_\infty - \frac{R'_S(f_S)}{2\pi f_S}\right] F(f) \quad ,$$

Eq. 45

where

$$F(f) = \frac{1}{\sqrt{1 + \left(\dfrac{f}{f_O}\right)^2}} \quad ,$$

Eq. 46

The estimated accuracy of the above closed-form expressions is better than 10%, for $0.2 < \frac{w}{h} < 5$, $0.001 < \frac{t}{w} < .02$ and $g > w + 2\,(h + t)$. The accuracy is defined here as the relative error in R' (or L') at a given frequency, or the relative error in frequency, for a given resistance (or inductance) per unit length, whichever is smaller.

SECTION 3

APPENDICES
PREVIOUS QUARTERLY REPORTS

3.1 Q4 1990 Quarterly Report

Section 1.0

Application of HTSC Interconnects for Digital Multi-Chip Modules

1.1. Technology Requirements and Opportunities

Since nearly the advent of integrated circuit technology, the vision has been to bypass the great expense and performance compromises of multi-level packaging by implementing entire systems (or major portions thereof) on a single IC wafer. Unfortunately, a number of technical realities mitigate against such a wafer-scale integration approach, at least for general purpose digital systems. The principal problem is yield, and the very high overhead costs of coping with this through redundancy, but perhaps equally important are issues of process and design optimization. Manufacturers of a specific ultra high density DRAM chip could not be expected to achieve the same cost, density and performance levels if the function had to be created as a part of a larger general-purpose logic design. These, and other, practical considerations have modified the focus away from the single semiconductor substrate wafer scale integration vision to the "hybrid wafer scale" concept in which virtually the same density goals are achieved in a multi-chip module (MCM) virtually "tiled" with VLSI die (as illustrated at the right of Fig. 1-1)

It is now generally accepted that the coming wave in electronics packaging is the multi-chip module (MCM). In MCM packaging technology, bare integrated circuit die are attached, both physically (chip bonded) and electrically (pad bonded), to a substrate which carries some type of multi-layer interconnect system to provide for the power connections to the die and the large number of signal interconnections required between the various chips on the MCM, and to the "outside world". The MCM, which may contain anywhere from a few IC chips to over a hundred in current MCM practice (and which may be expected to increase to many hundreds and possibly the low thousands in the future), represents the first-level package for the IC die. By eliminat-

ing the requirement for a large number of individual IC packages, the MCM allows for major reduction in size and weight in electronic systems (and potentially reduction of cost).

One of the key derivative benefits of MCM technology, which is a consequence of the reduction in size, is a major reduction of signal propagation delay or signal latency. In transmission lines, the propagation velocity of signal pulses is limited by the speed of light divided by the square root of the average dielectric constant of the dielectric(s) between the signal line and ground plane(s). The total pulse delay is, of course, not less than the line length divided by this velocity. The very small distances between IC chips in MCM's (as compared to circuit board packaging) greatly reduced this propagation delay. Since in most digital systems the maximum clock frequency is limited to the reciprocal of the sum of the logic circuit delay plus this signal interconnect propagation delay, reduced propagation delays translate into higher system speeds, particularly if the logic speeds can be increased as well. Of course, the major direction of thrust in the semiconductor/IC industry has been to increase chip speeds (the new MacIntosh FX runs at a 40 MHz clock rate, for example), so that the reduced interconnect delays afforded by MCMs are precisely what digital system designers need to translate the escalating IC speeds into greatly improved system performance.

1.2. Constraints on MCMs Due to Interconnect Resistance

The simplest concept for a large MCM would be to use normal semiconductor processing (two to four layers of metal interconnects with typically $\approx 1\mu m$ signal linewidths) on a large (4" to 6" or larger) wafer to serve as the inter-chip connection medium in the MCM. Unfortunately, even a 4" square MCM would have up to 8" long signal lines, which, assuming a $1\mu m \times 0.5\,\mu m$ cross section and a $\rho = 1.7 \times 10^{-6}$ ohm cm metal resistivity (copper; aluminum would be worse), the line resistance would be $R_{max} = 6909$ ohms. This is two or three orders of magnitude too large to be useable for interconnects in a high speed digital system.

All signal interconnects in digital systems are, for better or for worse, transmission lines. As illustrated in Fig. 1-2, signal lines implemented with normal metal conductors can usually be approximated as an ideal distributed L-C line with a conductor resistance in series with each inductor (this ignores the dielectric losses). In the ideal case when the total signal line resistance is very small in comparison to the line impedance, $R_{line} << Z_o$, the waveform integrity is excellent and the velocity of propagation, v_p, is just given by

$$v_p = c / \sqrt{\varepsilon_r} \qquad \text{Eq. 1}$$

where ε_r is the average dielectric constant in the line. Since the line impedances normally employed are in the range of $Z_o = 50\Omega$ (or within a factor of 2 of this), clearly the 8" long, W = 1μm copper line ($R_{line} = 6909\Omega$) case cited above is far from this ideal case. As noted at the bottom of Fig. 1-2, for $R_{line} << Z_o$, the propagation approaches a distributed R-C line characteristic which exhibits so-called "telegrapher's delay" or signal "diffusion" characteristics, with gross distortion, risetime degradation and long signal delays.

While we know line resistances of a few ohms are great and a few kilohms are terrible, we would like to be a bit more quantitative as to what line resistance is tolerable in practical applications. The signal interconnect configuration which is most tolerant of line resistance is the source-terminated, open-load case, as approximated by CMOS. Clearly, $R_{line} < 10\Omega$ is nearly ideal and $R_{line} > 200\Omega$ is very bad, with long delays to reach threshold and very poor risetimes. Practically, $R_{line} = 50\Omega$ is useable for this case, and $R_{line} = 100\Omega$ might be tolerable if the gross reduction of slew rate through threshold is acceptable (as it might be for data lines, but not for a clock, for example). In the more common, load-terminated, configuration as used with ECL and most GaAs ICs to implement very high speed systems, the line resistance tolerance is less. When single-ended signal transmission is used with a logic voltage threshold (V_{BB}) reference internal to the receiving chip, the dc attenuation of the signal "high" due to the line resistance/load resistor voltage divider directly degrades the noise margin on a signal high. The most favorable case ($R_{source} = Z_o = 50\Omega$), in which an $R_{line} = 15\Omega$ might be acceptable. In most practical load-terminated cases, however, the

source resistance is much lower, increasing the sensitivity to conductor resistance and making $R_{line} = 10\Omega$ about the practical maximum. If full-differential signal transmission were used for this ECL case, the tolerance would be similar to the CMOS case.

Note that pulse propagation involves, for fast signal risetimes, reasonably high frequency signal components. For example, in a 100 MHz clock rate system, at least 300 MHz (3rd harmonic) frequency components are important and must be minimally attenuated to avoid pulse distortion, risetime degradation and excess delay. In room temperature copper at 300 MHz, the skin depth (thickness of the surface region in which the AC current is carried) is only $\delta = 3.8\,\mu$m. or $R_S = 4.6$ milliohms per square. Hence, for a conductor of width W and thickness t_m, for $t_m \sim 2$ delta , instead of behaving as if its conducting area were $A_W = t_m W$, it will effectively be less than $(A_W)_{ac} = 2\delta\,(W + t_m)$, which may be much smaller, and frequency-dependent, as δ is proportional to $1/\sqrt{f}$. Hence, a simple dc analysis substantially underestimates the seriousness of the line resistance problem with normal metal interconnects.

1.3. Interconnect Conductor Resistivity Influence On MCM Fabricability

Understanding that the signal interconnect conductor resistances) must be kept under 10 ohms or so (for ECL-type signal, perhaps five to ten times this for CMOS), we would like to quantitatively evaluate the implications for the resistivity of the conductor metal on the practical realizability of high density multi-chip modules. We will assume, for simplicity, a square MCM with N_R rows and columns of chips (for a total of $N_{chip} = N_R^2$ VLSI die on the MCM) with the die mounted as closely as their mounting technology allows (about 0.35 mm die separation for flip-chip mounting or about 2mm die separation for wirebonding). The total MCM size, X_M, is N_R times the sum of the chip size plus this die separation. The maximum length of a signal interconnect (corner to corner) will be taken as $2X_M$ (Manhattan wiring with no wrong-direction paths). To keep the conductor resistance, R_{max}, of such a worst case signal line below the allowable limit for proper signal propagation characteristics (eg., R_{max} 10Ω) given a finite conductor resistivity, ρ, requires that the cross-sectional areas, and

hence (assuming a constant thickness to width ratio, T_{WR} for the wires) the conductor linewidth, W, must be kept adequately large. Hence as the MCM size, X_M and the metal resistivity, ρ, are increased, W must be increased as $\sqrt{\rho X_M}$. Unfortunately, increasing W decreases proportionately the length of wire we can implement on one layer of interconnect. The only way around this is to increase the number of signal layers, S, used to implement the multi-layer interconnects in the MCM.

While conceptually one may arbitrarily increase the numbers of signals interconnect layers, S, used to implement an MCM in order to match the requirements for inter-chip interconnect wiring, these are very real practical constraints on S. As W is increased, in order to maintain the desired Z_o ($\approx 50\Omega$, the stripline dielectric thicknesses must also be increased, which, if many layers, S, are required can make the total multi-layer interconnect structures thickness impractical. Automatic place and route software packages are also generally unable to cope with more than 6 or 8 signal layers in most commercial packages (although propriety packages for internal use allowing more layers likely exist). Further, in a multi-layer interconnect scheme of the usual $triplate_k$ (ground-X-Y-ground) configuration, adding 2 signal layers means adding 3 more total metal layer masks plus 3 more inter-layer via masks (one through each of the 3 added dielectric layers). Processing yields tend to fall as the yield per mask level taken to the power of the number of mask levels. Hence while it may sound vaguely credible to say that it would take (at dc) S = 44 layers of copper interconnects to wire a 6" high density flip-chip MCM, when we note that this requires 67 total metal layers (including grounds) or a total of 133 mask steps (metal + via) to make such a structure (if you are a processing person you likely have passed out at this point), you have only to note that even a 95% full-wafer (MCM substrate) yield per mask step would give a $0.95^{133} = 0.109\%$ estimated end yield for the (very expensive) process. While, through the use of in-process and post-fabrication EC (engineering change) rework capabilities, useable production yields of some very complex multi-layer ceramic boards have been demonstrated (eg. IBM), the fact that implementing large numbers of signal interconnect layers is extremely difficult and expensive and represents a major technological obstacle to increasing maximal density MCM sizes.

1.4. Quantitative Comparison Of Normal Metal And HTSC MCM Implementations

While it is clear from a qualitative standpoint that interconnect metal resistivity requires larger numbers of interconnect layers to wire an MCM, and from a technology standpoint that too many layers is impractical we need a quantitative analysis to determine if HTSC technology is required for real cases of interest for high density MCMs. Such a quantitative MCM wireability analysis will have a result, for example, the determination of how many signal interconnect layers are required to complete the inter-chip wiring on a given sized maximal density MCM substrate. Fig. 1-3 gives an overview of how such a wireability analysis is carried out, with Fig. 1-4 describing the detailed equations and relationships involved. As shown in Figs. 1-3 and 1-4, the essence of the analysis is to equate the wire supply (right hand side of the figures), as determined from the interconnect linewidth, W, and number of interconnect layers, S, with the amount of wire anticipated to be required to complete all of the signal interconnects on the MCM. While we have discussed the effect of conductor resistivity, ρ on W and other aspects of the supply side of Figs. 1-3 and 4, we must now give our attention to the demand (left) side.

Obviously, the total wire demand, or total amount of wire required to complete the inter-chip MCM wiring will be the total number of wires required (which is approximately the total number of pads on all ICs divided by 2) times the average length of the wires (see Fig.1-4 for details). An important tool illuminating both the required number of pads per chip and the average wire length is the empirical relationship identified by Rent at IBM relating the number of I/O pins, I, required at a package level to the number of circuits, N_g, contained within it as

$$I = BN_g^p \qquad \text{(Rent's Rule)} \qquad \text{Eq. 2}$$

where the Rent's exponent, p is typically of the order of 2/3 (0.5 to 0.7; see, for examples, Ref. 1 and 2). As shown in Fig. 1-1 through 1-5 of Ref. 1, while some kinds of IC's (particularly memory chips) have substantially fewer I/O's than suggested by Eq. 2, for general high performance logic chips (such as gate arrays or standard cell

arrays), an N_g = 10K gate chip would be expected to have about 370 I/O pads, while a 30K gate chip would have about I = 700 pads. In fact, these numbers are generally realizable only if the die are flip-chip mounted (area array pads); with conventional wirebonding, pad to pad spacing limitations (4 mils center to center for conventional, or about 3 mils for staggered pads, in current wirebonding technology) also apply. Hence, while a 1 cm 30K gate chip would "want", from Rent's Rule, about 700 pads, there is only room, at 4 mil spacing, for 400 peripheral pads (or about 530 staggered pads at 3 mils spacing).

To evaluate the total wire length, we need not only the total number of wires ($\approx N_{pads}/2$), but also the average wire length, $\bar{L}$ which is usually written as $\bar{L} = \bar{R}X_{chip}$, where X_{chip} is the chip pitch and $\bar{R}$ is the average wire length measured in chip pitches. $\bar{R}$ must be obtained from some type of statistical wire length theory. A very simple theory is obtained if we assume that the chips are randomly placed on the MCM so that it would be equally probable that a given chip would connect to any other chip location. For this random placement case, it can be show that $\bar{R} = 2N_R/3$, where N_R is the number of rows and columns of chips. This is a quite pessimistic model, however, since it is the goal of intelligent chip placement to make as many of the interconnects as possible as short as possible. Based on applying the Rents Rule (Eq. 2) concept to progressive subdivisions of the system, Donath developed an expression for $\bar{R}$ involving the total number of chips, $N_{chip} = N_R^2$ and the Rent's Rule exponent, p (see Eq. A-8, p.64, of Ref. 2, or the bottom left side of Fig. 1-4 here for the somewhat complicated expression for $\bar{R}$). For N_{chip} = 4 (N_R = 2), the Donath theory gives the same result ($\bar{R}$ = 4/3) as the random placement case, which is reasonable as all chips are virtually nearest neighbors. For purposes of the copper HTSC comparisons in Figs. 1-5 through 1-8, a Rent's exponent value of p = 2/3 was used.

Fig. 1-6 summarizes the calculation assumptions (values of parameters in Fig. 1-4) for a maximal density MCM with up to N_R = 40 rows and columns of flip-chip mounted, 0.6 cm 10K gate VLSI die (I = 370 signal I/O pads) mounted on it. The calculation in for the number of copper interconnect layers, S, necessary to keep the maximum line resistance, R_{MAX}, below both for dc and for 300 MHz ac frequency components (eg.

the 3rd harmonic of a 100 MHz check) 10 ohms both for dc and for 300 MHz are frequency components (eg., the 3rd harmonic of a 100 MHz check. As seen in Fig. 1-6, with N_R = 24 rows and columns of die (576 chips), the MCM size will be X_M = 6" and will require over S_{dc} = 43 layers of W = 32 μm linewidth copper interconnect at dc, or for 300 MHz ac, S_{ac} = 61 layers of W = 45.6 μm copper lines. On the other hand, assuming that the same (or probably better) signal propagation quality can be obtained with W = 2 μmwide HTSC lines, the calculated number of interconnect layers in Fig. 1-8 is only s = 2.68. In other words, if the HTSC linewidth were reduced to W = 1.5 μm, the whole MCM could be wired with only 2 HTSC signal layers. This is a vast improvement over 61 copper signal interconnect layers (or more relevantly, 93 total metal layers including ground planes). These ac and dc results are plotted versus MCM size in Fig. 1-5. Figs. 1-7 and 1-8 show the dc only results and plots for a similar case using larger, 1cm 30K gate chips with 700 signal I/O pads, also flip-chip mounted. Numerous other cases have been analyzed, with all of them showing substantial to dramatic advantages for HTSC interconnects as the MCM sizes increase.

As is obvious from the foregoing discussion, and Figs. 1-5 through 1-8, there is a strong need for an HTSC multi-layer interconnect technology in order to practically implement large maximal density MCMs having large numbers of high I/O count VLSI die. Having established the need for HTSC materials in MCMs, the next issue is the requirements on the HTSC technology to effectively address these needs. One very important issue is the dielectric. For the system to operate at a clock frequency approaching the maximum clock frequency of the IC's the interconnect propagation delay, t_{pd} must be small in comparison to t_{logic}. Typically, where maximum performance is desired, an effort will be made to keep t_{pd} to 20 percent or so of the clock cycle time, $t_{clock} = 1/f_c$. Hence, for an f_c = 100 MHz clock frequency, we would like a worst case interconnect delay of 20 percent of 10ns or t_{pd} = 2 ns. For a 6" MCM with a longest case L = 12" line, this would require an electromagnetic propagation velocity, v_p, of v_p = 15.24 cm/ns or a unit delay of $1/v_p$ = 167 ps/inch. For a lossless interconnect line fully imbedded in a dielectric (eg. stripline configuration) of relative dielectric constant ε_r from Eq. 1, this would require that the dielectric constant cannot exceed ε_r = 3.9. Clearly this excludes the use of the usual $LaAlO_3$ HTSC

growth substrates (ε_r = 26) as the signal interconnect dielectric, as its stripline velocity (v_p = 5.88 cm/ns or $1/v_p$ = 432 ps/inch) is several times slower than desired and would make this worst-case line delay, t_{pd}, over half of the 100 MHz clock period, an unacceptable performance penalty. Dielectrics such as silicon dioxide (ε_r = 3.9) and many polyimides would be acceptable (although the corrosive nature of some polyimides, might destroy the HTSC materials), but a low dielectric constant polymer such as benzocyclobutene (BCB) with ε_r = 2.65 (v_p = 18.42 cm/ns or $1/v_p$ = 138 ps/inch) would be better (and BCB is low-loss and non-corrosive in nature, so it might be less likely to degrade the HTSC conductors) Fig. 1-9 shows the variation of the unit delay $1/v_p$, of transmission lines as a function of ε_r. While $\varepsilon_r \leq 4$ values are certainly desirable, if MgO - like or C_aF_2 - like dielectric constants ($\varepsilon_r \approx 9$ or less) were necessitated by the HTSC technology, this would probably be acceptable.

Another critical issue from the standpoint of HTSC technology is the pulsed current densities that the signal interconnect lines must support. These are shown in Fig. 1-10 for both the case of load-terminated (ECL or GaAs) and source - terminated, open load (CMOS - like) transmission line interconnects. For ECL or GaAs, the peak currents required are about 22 ma, with a dc component present, while 5V CMOS requires ±50 ma pulses (of duration 2 t_{pd}), pure ac. If we assume a 1μm × 2μm HTSC conductor, the pulsed current densities are respectively 1.1×10^6 A/cm^2 and 2.5×10^6A/cm^2. While these pulse values cannot be directly related to the dc critical current density value, J_c, dc J_c values substantially higher than these numbers have been demonstrated in high quality HTSC films. It is also worth noting that the loss of the pure superconducting state in most HTSC materials is somewhat "soft" near J_c, and for this application, the interconnect conductor need not have zero resistance (several ohms is certainly OK), allowing for higher current density operation.

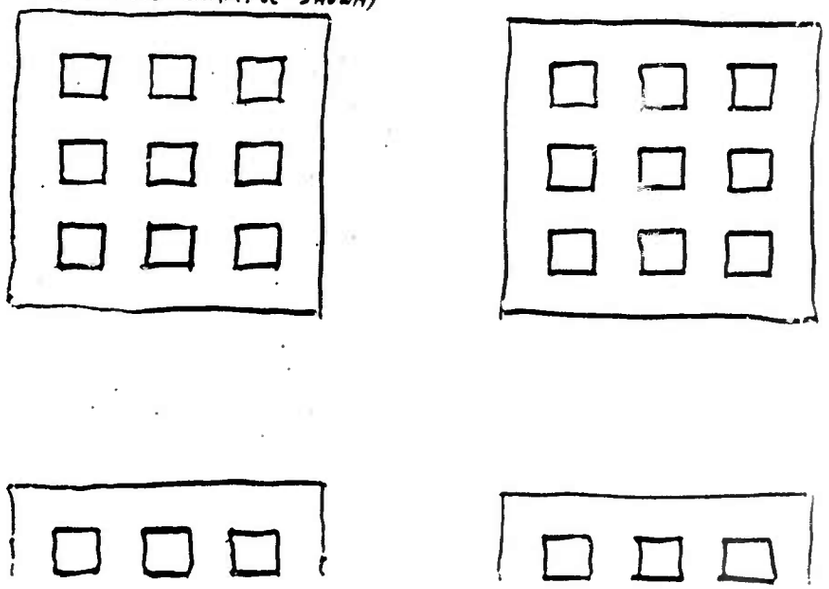
References

1. Rao R. Tummala & E.J. Rymaszewski (Editors), "Microelectronics Packaging Handbook" Van Nostrand Reinhold, 1989 (ISBN 0-442-20578-3).

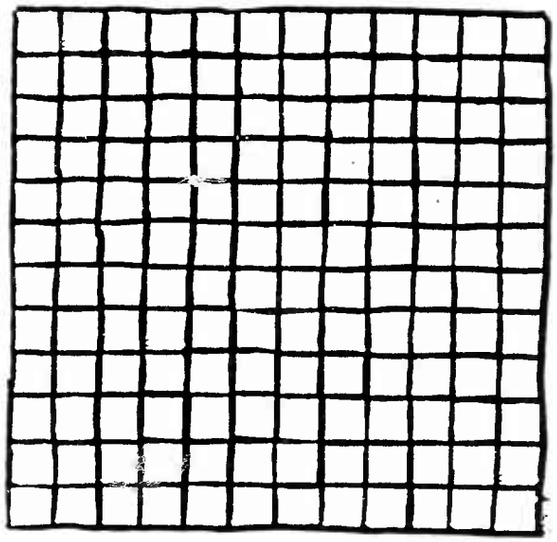
2. Donald P. Seraphim, Ronald C. Lasky and Chi-Yu Li (Editors), "Principles of Electronic Packaging", McGraw-Hill Book Company, 1989 (ISBN 0-07-056306-3).

MANY CONVENTIONAL MCMs

(16 FOR EXAMPLE SHOWN)



MAXIMUM DENSITY HTSC MCM



MANY MCMs

HIGH 2nd-LEVEL PACKAGE COST

LONG MCM to MCM DELAYS

MODEST WIRING AND POWER DENSITIES

REDUCED COST →

MAXIMUM SPEED →

ONE OR FEW MCMs

MINIMAL 2nd-LEVEL PACKAGE COST

SHORT DELAYS WITHIN MCM

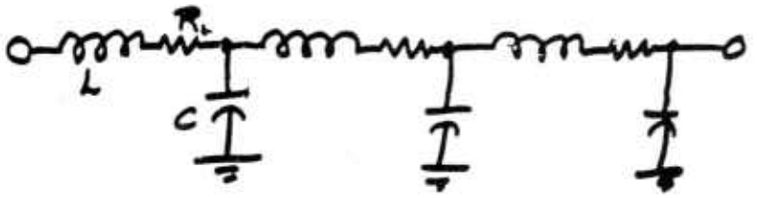
HIGH WIRING AND POWER DENSITIES

(REQUIRES HTSC INTERCONNECTS TO ACHIEVE INTER-CHIP CONNECTIVITY WITH PRACTICAL NUMBER OF SIGNAL LAYERS)

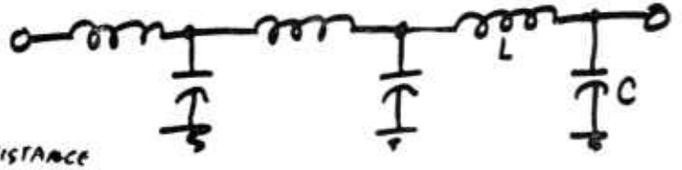
Figure 1-1

SIGNAL PROPAGATION ON NORMAL METAL LINES

LOSSY LINE MODEL



FOR $R_{LINE} << Z_0$



$R_{LINE} = \frac{\rho}{A} L_L$ ← dc RESISTANCE

$\frac{\rho}{A}$: RESISTANCE PER UNIT LENGTH

L_L: TOTAL LENGTH OF LINE

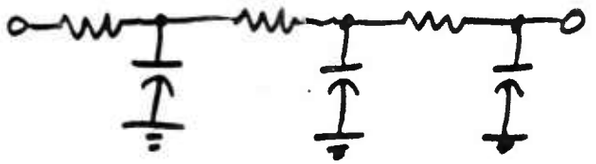
$X = V_p \tau$

$V_p = \frac{1}{\sqrt{LC}} = \frac{c}{\sqrt{\epsilon_r}}$ ← SPEED OF LIGHT

WAVEFORM PRESERVED

} IDEAL

FOR $R_{LINE} >> Z_0$



SIGNAL "DIFFUSES" DOWN DISTRIBUTED RC RATHER THAN NORMAL PROPAGATION.

$X = \sqrt{D\tau}$

HIGHLY DISTORTING, VERY SLOW RISETIMES, LONG PHASE DELAYS, DISPERSIVE.

} VERY BAD FOR RISETIME DELAY

WE WANT $R_{LINE} < Z_0$ (PREFERABLY $R_{LINE} << Z_0$)

Figure 1-2

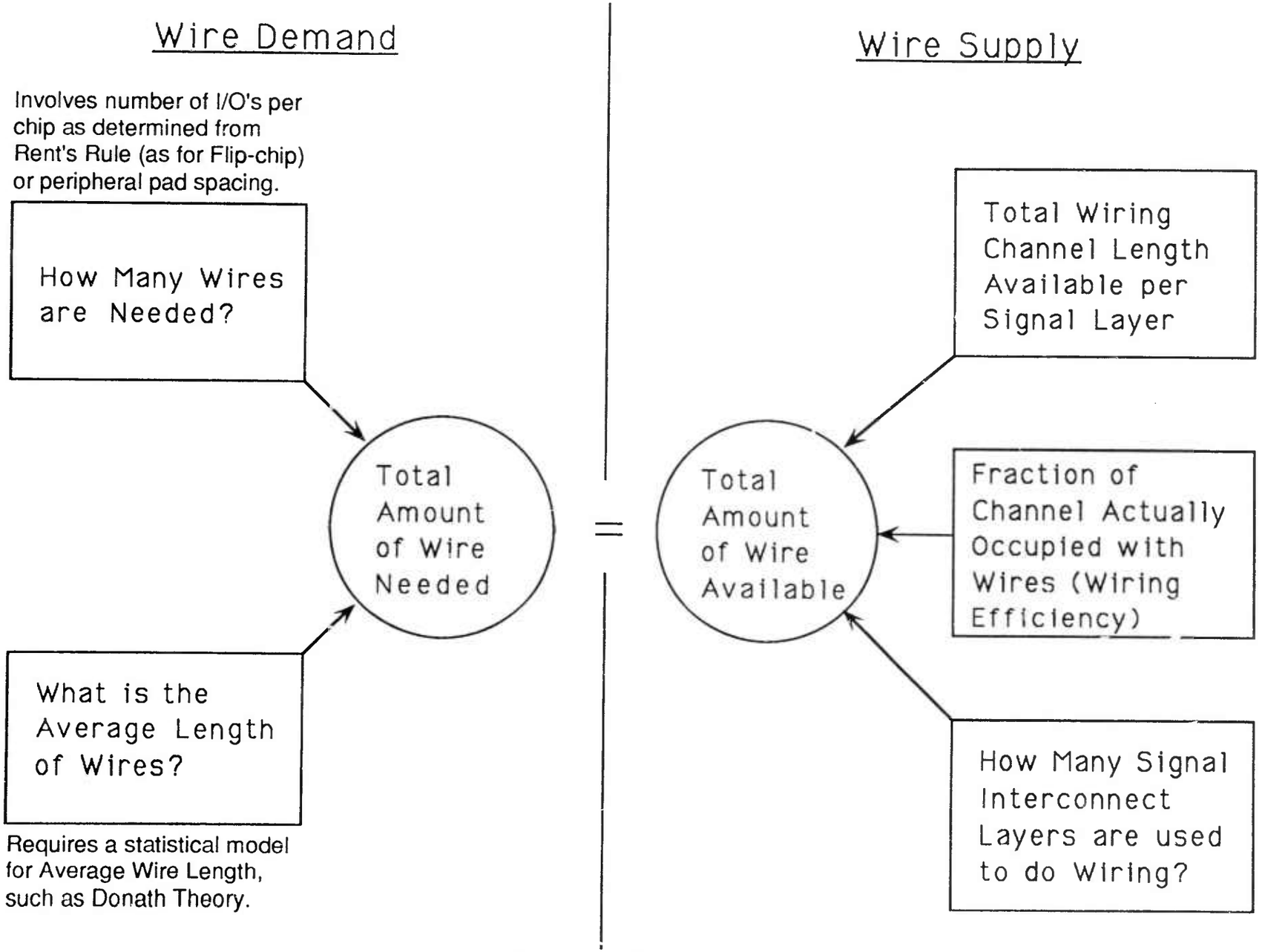

Wire Demand
Involves number of I/O's per chip as determined from Rent's Rule (as for Flip-chip) or peripheral pad spacing.
How Many Wires are Needed?
Total Amount of Wire Needed
What is the Average Length of Wires?
Requires a statistical model for Average Wire Length, such as Donath Theory.
=
Wire Supply
Total Wiring Channel Length Available per Signal Layer
Total Amount of Wire Available
Fraction of Channel Actually Occupied with Wires (Wiring Efficiency)
How Many Signal Interconnect Layers are used to do Wiring?

Figure 1-3

WIRING DEMAND

Pitch On Which Chips Are Mounted, X_{chip}
(From Chip Size And Minimum Spacing)

Number Of Rows (= # Columns) Of Chips, N_R

Overall Size Of MCM, $X_{MCM} = N_R X_{chip}$

Total Number Of Chips, $N_{chips} = N_R^2$

Number Of Signal I/O's Per Chip I
(From Rent's Rule Or Peripheral Pad Space)

Total Number Of Pads, $N_{pads} = N_R^2 I$

Average Number Of Pads Per Net, P_N
$P_N \approx 2$ For Point To Point, $P_N \approx 3$ For "Stitched"

Total Number Of Wires, $N_W = \frac{(P_N - 1)}{P_N} N_{pads}$

$$N_W = \frac{(P_N - 1)}{P_N} N_R^2 I$$

Total Length Of Wire Required $L_{R\,total} = \bar{L} N_W$

Where $\bar{L}$ Is Average Wire Length, $\bar{L} = \bar{R} X_{chip}$
(Where $\bar{R}$ Is Average Wire Length In Chip Pitches)

$\bar{R}$ Must Be Obtained From A Statistical Wire Length Theory

Random Chip Placement $\bar{R}_{RND} = \frac{2}{3} N_R$

Donath Theory For Wire Length

$$\bar{R}_{Donath} = \frac{2}{9}\left[7\frac{N_{chip}^{p-.05}-1}{4^{p-0.5}-1} - \frac{1-N_{chip}^{p-1.5}}{1-4^{p-1.5}}\right]\frac{1-4^{p-1}}{1-N_{chip}^{p-1}}$$

Where p Is Rent's Rule Exponent

Equating

$L_{R\,total} = L_{A\,total}$

$$\bar{R} X_{chip}\left(\frac{P_N - 1}{P_N}\right) N_R^2 I = \eta \frac{S N_R^2 X_{chip}^2}{P_{WR} W}$$

Gives For Required # Layers, S:

$$S = \left[\left(\frac{P_N - 1}{P_N}\right)\frac{P_{WR}}{\eta}\right]\frac{\bar{R} I W}{X_{chip}}$$

Figure 1-4

WIRING SUPPLY

Width Of Metal Signal Lines = W

Thicknesss Of Signal Lines Metal $t_m = T_{WR} W$

Where T_{WR} = Thickness To Width Ratio (= 0.5 TYP)

Area Of Signal Line $A_W = W t_m = T_{WR} W^2$

Maximum (corner to corner) Line Length, $L_{MAX} = 2X_{MCM}$

Metal Resisitivity = ρ

Resistance Of Max Length Wire, $R_{MAX} = \frac{\rho}{A} L_{MAX}$

or $R_{MAX} = \frac{2\rho X_{MCM}}{T_{WR} W^2}$

Minimum Signal Line Width, $W = \sqrt{\frac{2\rho X_{MCM}}{R_{MAX} T_{WR}}}$

Crosstalk - Limited Pitch To Width Ratio, P_{WR}

Minimum Signal Line Pitch, $X_{WP} = P_{WR} W$

Maximum Length Of One Wire Channel = X_M

Maximum Number Of Channels Per Layer, $N_{CH} = \frac{X_M}{X_{WP}}$

Maximum Channel Length Per Signal Layer, $L_{CPL} = N_{CH} X_M = \frac{X_M^2}{X_{WP}}$

Total Number Of Signal Layers = S

Total Channel Capaciy (Length For All Layers) $L_{CT} = S\frac{X_M^2}{X_{WP}}$
(This Is Typically Noted In Inches Per Square Inch)

Wiring Efficiency (Fraction Of Channel With Wire) = η

Total Available Wire Length, $L_{A\,total} = \eta S \frac{X_M^2}{X_P}$

or $L_{A\,total} = \eta S \frac{N_R^2 X_{chip}^2}{P_{WR} N}$

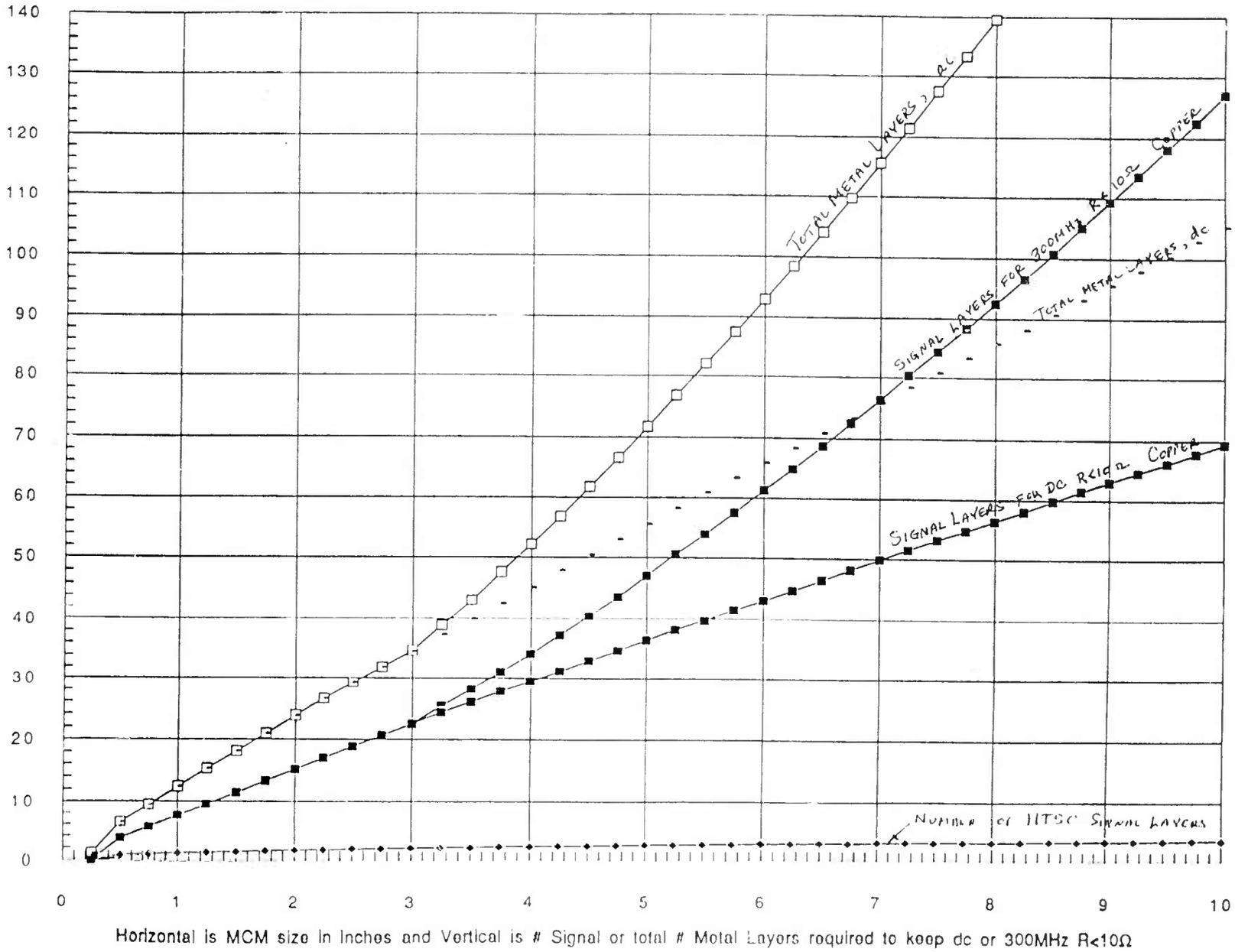
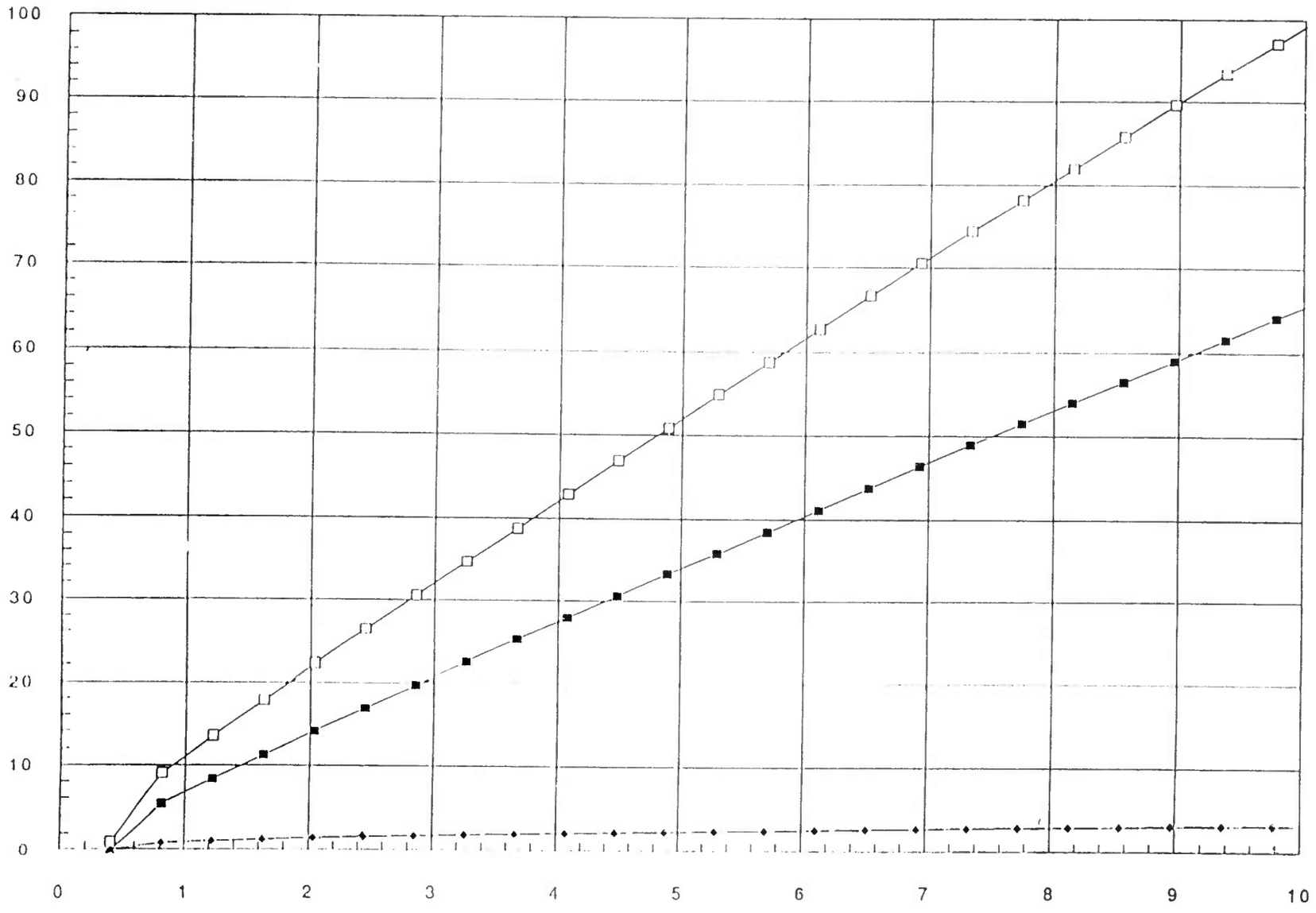

fc10K SH ac/dc p=0.667 Rmax=10Ω dc and 300MHz Comparison of MCM w W=2.0μm HTSC vs. Cu Lines, Donath model, 370 I/O 10Kgate 0.6cm Chips
140
130
120
110
100
90
80
70
60
50
40
30
20
10
0
0
1
2
3
4
5
6
7
8
9
10
TOTAL METAL LAYERS, AC
SIGNAL LAYERS FOR 300MHz R≤10Ω COPPER
TOTAL METAL LAYERS, dc
SIGNAL LAYERS FOR DC R≤10Ω COPPER
NUMBER OF HTSC SIGNAL LAYERS
Horizontal is MCM size in Inches and Vertical is # Signal or total # Metal Layers required to keep dc or 300MHz R<10Ω

Figure 1-5

	A	B	C	D	F	H	I	J	K	L	M
1	AC (Skin Effect) Calculation at Freq= 300 MHz										
2	10 Kgate Flip-Chip Rmax= 10 vs. HTSC with W= 2.0 µm Linewidth										
3	Comparison of # Signal Layers Req'd on MCM for HTSC vs. Donath's theory and Rent's rule p										
4	Array assumed square with NR rows and NR Columns and NC=NR^2 Chips										
5											
6	Skin Depth, DELTA= 3.788645433014354D-04 cm. Current Distribution Form Factor taken as FF= 1										
7	The Rent's Rule exponent assumed in this calculation is p= .667										
8	10 Kgate Flip-Chip of Xc= .6 cm square with Xg= .035 cm gaps between chips for a Xp= .6350 mounting pitch.										
9	IOP= 370 I/O Pads per chip										
10	Pn= 2 (# Pad conns. per wire), Weff= .4000 (wiring efficiency), and signal line pitch to w ratio= 4										
11	Conductor resistivity= 1.70D-06 ohm-cm, with thickness to width ratio of WTR= .5										
12	NC is the total number of chips on the MCM (=NR^2) and Rbar is the average wire length (in pitches)										
13	XM is the overall size of the square MCM in cm, and S is the # sig layers req'd to keep R of a 2*XM line <Rmax										
14	Rmax= 10 ohms Maximum Line Resistance Allowed for Longest (L=2*XM) Line.										
15											
16	NR=	NC=	Rbar=	XM (cm)	XW (cm)	XM (inches)	S (ac Copper)	S (HTSC)	MT (ac total M)	S (dc Copper)	MT (dc Copper)
17	1	1	0	0.635	0	0.25	0	0	1	0	1
18	2	4	1.333333	1.27	0.0009293	0.5	3.609882	0.7769029	6.414823	3.609882	6.414823
19	3	9	1.692126	1.905	0.00113816	0.75	5.6109	0.9859629	9.41635	5.6109	9.41635
20	4	16	1.977663	2.54	0.00131423	1	7.572191	1.152339	12.3582865	7.572191	12.3582865
21	5	25	2.219835	3.175	0.00146935	1.25	9.502656	1.293447	15.253984	9.502656	15.253984
22	6	36	2.432605	3.81	0.0016096	1.5	11.4074	1.417423	18.1111	11.4074	18.1111
23	7	49	2.62381	4.445	0.00173856	1.75	13.28987	1.528834	20.934805	13.28987	20.934805
24	8	64	2.798363	5.08	0.0018586	2	15.15264	1.630542	23.72896	15.15284	23.72896
25	9	81	2.959578	5.715	0.00197135	2.25	16.99771	1.724478	26.496565	16.99771	26.496565
26	10	100	3.109811	6.35	0.00207798	2.5	18.82666	1.812016	29.23099	18.82666	29.23099
27	11	121	3.250811	6.985	0.0021794	2.75	20.64084	1.894173	31.96126	20.64084	31.96126
28	12	144	3.383914	7.62	0.00227944	3	22.47222	1.971729	34.70833	22.44136	34.66204
29	13	169	3.510165	8.255	0.0024694	3.25	25.2532	2.045293	38.8798	24.22917	37.343755
30	14	196	3.630407	8.89	0.00265935	3.5	28.12735	2.115355	43.191025	26.00511	40.007665
31	15	225	3.745322	9.525	0.0028493	3.75	31.09037	2.182314	47.635555	27.76989	42.654835
32	16	256	3.855478	10.16	0.00303926	4	34.13843	2.246499	52.207645	29.52415	45.286225
33	17	289	3.961348	10.795	0.00322921	4.25	37.2681	2.308187	56.90215	31.26848	47.90272
34	18	324	4.063335	11.43	0.00341916	4.5	40.47628	2.367613	61.71442	33.00337	50.505055
35	19	361	4.161786	12.065	0.00360912	4.75	43.76014	2.424977	66.64021	34.72928	53.00302
36	20	400	4.256096	12.7	0.00379907	5	47.11711	2.480454	71.675665	36.44664	55.66996
37	21	441	4.346225	13.335	0.00398903	5.25	50.54402	2.534194	76.81723	38.15503	58.233745
38	22	484	4.438701	13.97	0.00417898	5.5	54.04108	2.58633	82.06162	39.85718	60.78577
39	23	529	4.525624	14.605	0.00436893	5.75	57.60388	2.636978	87.40582	41.55102	63.32653
40	24	576	4.610172	15.24	0.00455889	6	61.23135	2.686242	92.847025	43.23765	65.856475
41	25	625	4.692504	15.875	0.00474884	6.25	64.92174	2.734215	98.38261	44.91734	68.37601
42	26	676	4.772762	16.51	0.00493879	6.5	68.67341	2.78098	104.010115	46.59033	70.885495
43	27	729	4.851075	17.145	0.00512875	6.75	72.48483	2.82661	109.727245	48.25687	73.385305
44	28	784	4.927557	17.78	0.0053187	7	76.35458	2.871175	115.53187	49.91717	75.875755
45	29	841	5.002315	18.415	0.00550865	7.25	80.2813	2.914734	121.42105	51.57144	78.35716
46	30	900	5.075442	19.05	0.00569861	7.5	84.26371	2.957344	127.395565	53.21987	80.829805
47	31	961	5.147028	19.685	0.00588856	7.75	88.30061	2.999056	133.450915	54.86264	83.29396
48	32	1024	5.217153	20.32	0.00607851	8	92.39085	3.039916	139.586275	56.49992	85.74988
49	33	1089	5.285889	20.955	0.00626847	8.25	96.53335	3.079966	145.800025	58.13187	88.197805
50	34	1156	5.353304	21.59	0.00645842	8.5	100.7271	3.119248	152.09065	59.75863	90.637945
51	35	1225	5.419461	22.225	0.00664838	8.75	104.9711	3.157796	158.45565	61.38036	93.07054
52	36	1296	5.484419	22.86	0.00683833	9	109.2644	3.195645	164.8966	62.99719	95.495785
53	37	1369	5.54823	23.495	0.00702828	9.25	113.6061	3.232827	171.40915	64.60925	97.913875
54	38	1444	5.610945	24.13	0.00721824	9.5	117.9954	3.269389	177.9931	66.21664	100.32496
55	39	1521	5.672611	24.765	0.00740819	9.75	122.4315	3.3053	184.64725	67.8195	102.72925
56	40	1600	5.73327	25.4	0.00759814	10	126.9135	3.340645	191.37025	69.41794	105.12691

Figure 1-6

fc30K SH D p=0.667 R=10Ω Comparison of MCM wired with 2.0µm HTSC vs. Copper Lines with Rmax=10Ω ass. Donath model, 700 I/O 1cm 30Kgate Chips



Horizontal is MCM size in inches and Vertical is # Signal or total # Metal Layers Required to keep R<10Ω

Figure 1-7

fc30K SH D p=.667 R=10.Exl Comparison of 2μm HTSC MCM with Copper with R=10Ω limit

	A	B	C	D	E	H	I	J	K
1									
2									
3	30 Kgate Flip-Chip Rmax= 10 vs. HTSC with W= 2.000 μm Linewidth.								
4	Comparison of # Signal Layers Req'd on MCM for HTSC vs. Donath's theory and Rent's rule p								
5	Array assumed square with NR rows and NR Columns and NC=NR^2 Chips								
6									
7	The Rent's Rule exponent assumed in this calculation is p= .667								
8	30 Kgate Flip-Chip of Xc= 1 cm square with Xg= .035 cm gaps between chips for a Xp= 1.035 mounting pitch.								
9	IOP= 700 I/O Pads per chip								
10	Pn= 2 (# Pad conns. per wire), Weff= .40000 (wiring efficiency), and signal line pitch to w ratio= 4								
11	Conductor resistivity= 1.70μΩ-cm, with thickness to width ratio of WTR= .5								
12	NC is the total number of chips on the MCM (=NR^2) and Rbar is the average wire length (in pitches)								
13	XM is the overall size of the square MCM in cm, and S is the # sig layers req'd to keep R of a 2*XM line <Rmax								
14	Rmax= 10 ohms Maximum Line Resistance Allowed for Longest (L=2*XM) Line.								
15									
16	NR=	NC=	Rbar=	XM (cm	XW (cm)	XM (inches)	S (Copper)	MT (Total Lyrs)	S (HTSC)
17	1	1	0	1.035	0	0.40748031	0	1	0
18	2	4	1.333333	2.07	0.001186423	0.81496063	5.349412	9.024118	0.9017713
19	3	9	1.692126	3.105	0.001453066	1.22244094	8.31468	13.47202	1.144433
20	4	16	1.977663	4.14	0.001677856	1.62992126	11.22108	17.83162	1.33753
21	5	25	2.219835	5.175	0.0018759	2.03740157	14.08179	22.122685	1.501338
22	6	36	2.432605	6.21	0.002054945	2.44488189	16.90439	26.356585	1.64524
23	7	49	2.62381	7.245	0.002219595	2.8523622	19.69399	30.540985	1.774558
24	8	64	2.798363	8.28	0.002372846	3.25984252	22.4544	34.6816	1.892613
25	9	81	2.959578	9.315	0.002516784	3.66732283	25.18856	38.78284	2.001647
26	10	100	3.109811	10.35	0.002652923	4.07480315	27.89885	42.848275	2.103254
27	11	121	3.250811	11.385	0.002782409	4.48228346	30.58725	46.880875	2.198616
28	12	144	3.383914	12.42	0.002906131	4.88976378	33.2554	50.8831	2.288637
29	13	169	3.510165	13.455	0.003024797	5.29724409	35.90472	54.85708	2.374025
30	14	196	3.630407	14.49	0.003138981	5.70472441	38.53645	58.804675	2.455348
31	15	225	3.745322	15.525	0.003249154	6.11220472	41.15164	62.72746	2.533068
32	16	256	3.855478	16.56	0.003355711	6.51968504	43.75125	66.626875	2.607559
33	17	289	3.961348	17.595	0.003458988	6.92716535	46.33613	70.504195	2.679172
34	18	324	4.063335	18.63	0.003559269	7.33464567	48.90703	74.360545	2.74815
35	19	361	4.161786	19.665	0.003656802	7.74212598	51.46463	78.196945	2.814734
36	20	400	4.256996	20.7	0.003751799	8.1496063	54.00955	82.014325	2.879128
37	21	441	4.349225	21.735	0.00384445	8.55708661	56.54235	85.813525	2.941505
38	22	484	4.438701	22.77	0.003934921	8.96456693	59.06355	89.595325	3.00202
39	23	529	4.525624	23.805	0.004023357	9.37204724	61.57363	93.360445	3.060809
40	24	576	4.610172	24.84	0.004109891	9.77952756	64.07301	97.109515	3.117991
41	25	625	4.692504	25.875	0.00419464	10.1870079	66.5621	100.84315	3.173674
42	26	676	4.772762	26.91	0.00427771	10.5944882	69.04128	104.56192	3.227955
43	27	729	4.851075	27.945	0.004359197	11.0019685	71.51089	108.266335	3.28092
44	28	784	4.927557	28.98	0.004439189	11.4094488	73.97126	111.95689	3.332647
45	29	841	5.002315	30.015	0.004517765	11.8169291	76.42268	115.63402	3.383208
46	30	900	5.075442	31.05	0.004594997	12.2244094	78.86546	119.29819	3.432666
47	31	961	5.147028	32.085	0.004670953	12.6318898	81.29985	122.949775	3.481082
48	32	1024	5.217153	33.12	0.004745693	13.0393701	83.7261	126.58915	3.528509
49	33	1089	5.285889	34.155	0.004819274	13.4468504	86.14445	130.216675	3.574997
50	34	1156	5.353304	35.19	0.004891748	13.8543307	88.55512	133.83268	3.620592
51	35	1225	5.419461	36.225	0.004963164	14.261811	90.95833	137.437495	3.665336
52	36	1296	5.484419	37.26	0.005033567	14.6692913	93.35427	141.031405	3.709269
53	37	1369	5.54823	38.295	0.005102999	15.0767717	95.74314	144.61471	3.752426
54	38	1444	5.610945	39.33	0.005171499	15.484252	98.12511	148.187665	3.794842
55	39	1521	5.672611	40.365	0.005239103	15.8917323	100.5004	151.7506	3.836548
56	40	1600	5.73327	41.4	0.005305846	16.2992126	102.869	155.3035	3.877574
57									

Figure 1-8

R.C. EDEN

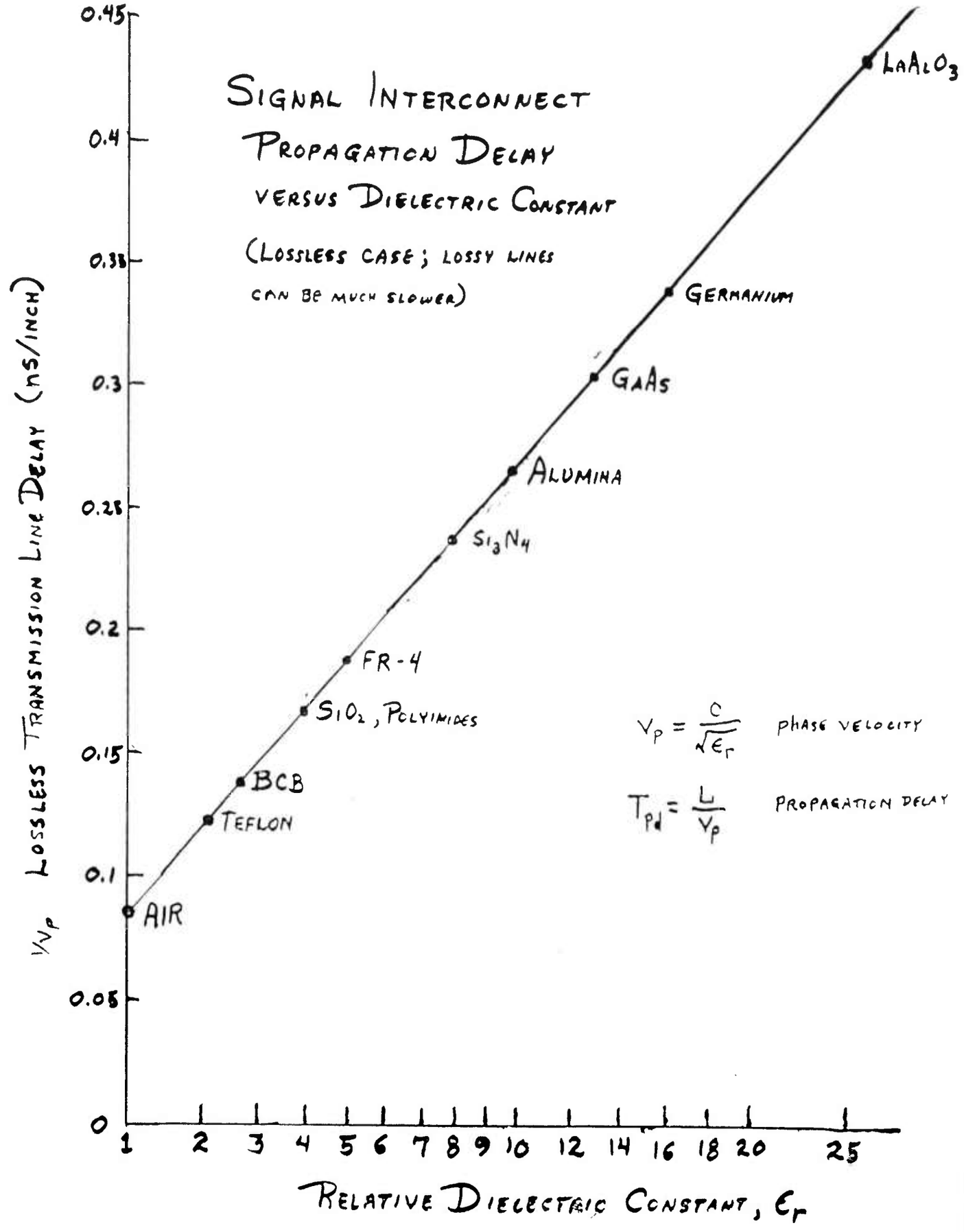
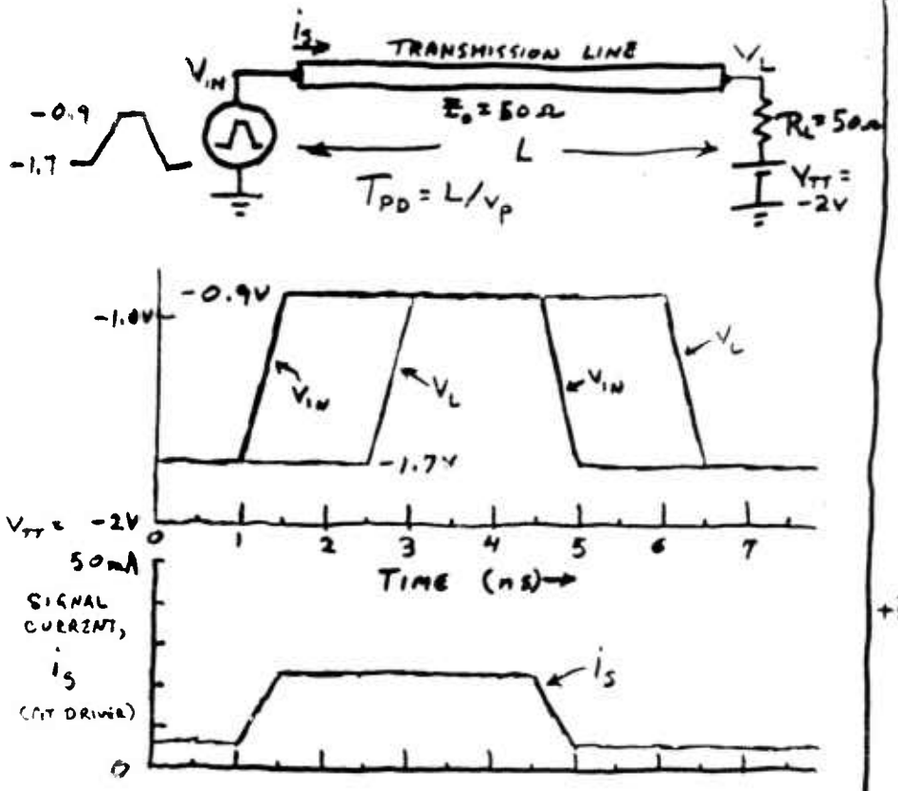


Figure 1-9

R. C. EDEN

CURRENT DENSITY REQUIREMENTS FOR SUPERCONDUCTING DIGITAL INTERCONNECTS

TYPICAL GaAs OR ECL
50Ω LOAD-TERMINATED LINE



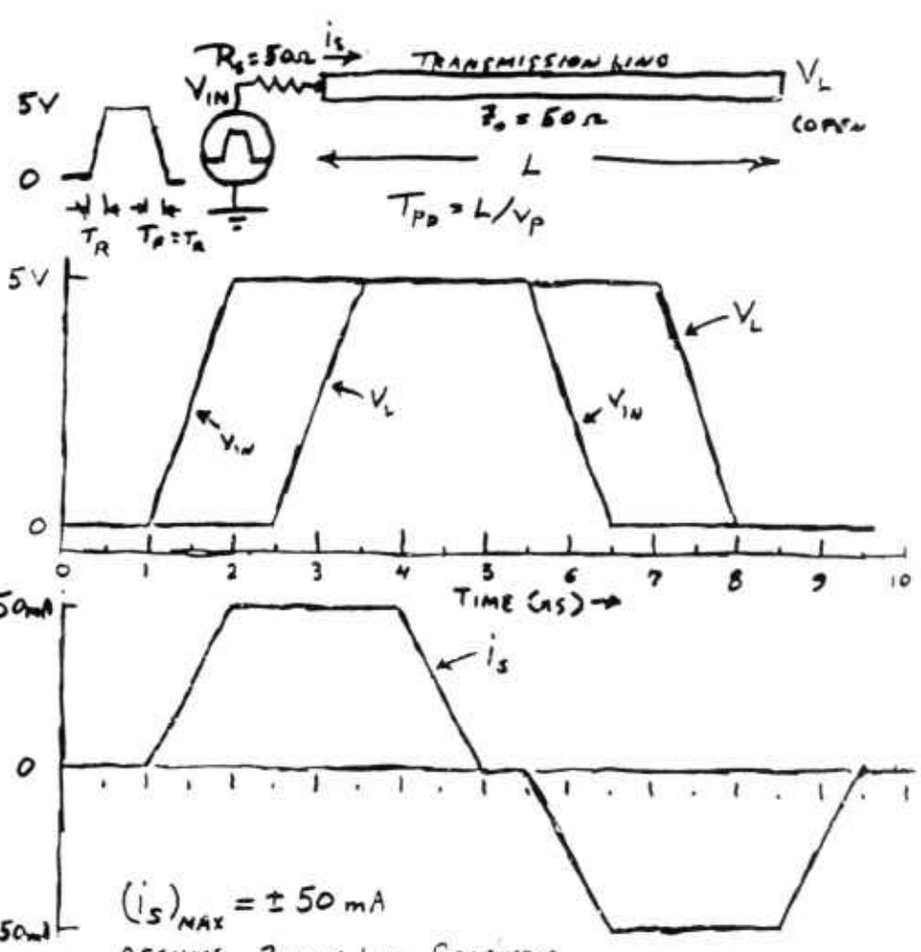
$(i_s)_{MAX} = 22\,mA$

ASSUME $2\mu m \times 1\mu m$ CONDUCTOR

$J_{MAX} = 22mA/2\times10^{-8}cm^2 = 1.1\times10^6\,A/cm^2$

LOAD CURRENT DC COMPONENT (WORST CASE SIGNAL) IS THIS LARGE, SO $J_c \geq 1.1\times10^6\,A/cm^2$

TYPICAL CMOS OR TTL
SOURCE-TERMINATED/OPEN LOAD



$(i_s)_{MAX} = \pm 50\,mA$

ASSUME $2\mu m \times 1\mu m$ CONDUCTOR

$J_{MAX} = 50\,mA/2\times10^{-8}cm^2 = 2.5\times10^6\,A/cm^2$

NOTE THAT LOAD CURRENT HAS NO dc COMPONENT, SO RELATION OF J_c TO J_{MAX} IS NOT CLEAR.

Figure 1-10

Section 2.0

Commercialization of High Temperature Superconducting Technology

2.1. Background

The HTSC program at DARPA is three years and approximately $75,000,000 has been spent in an effort to capitalize on what promised to be a high leverage HTSC technology for a variety of military and commercial applications. So far in electronics, only a small niche market has been identified and that is to apply HTSC for passive microwave devices. The total passive microwave device market is no larger than $50,000,000 per year with only a small portion of that, maybe $10,000,000 per year, will be used for HTSC; certainly no where close to justify the $25,000,000 per year that DARPA spends.

In the early days of HTSC discoveries, there was tremendous excitement in the technical and government communities about the potentials of HTSC. Even President Reagan made an appearance at a conference, closed to off-shore personnel, to highlight his enthusiasm and his support for this technology. The venture capitalists, by the droves, poured money to start-up enterprises, many of which had no products, no business plans, little knowledge of applications, or customers needs and in some cases even lacked the fundamentals of business know-how.

In the early days of this program, certainly no one had clear ideas as to where this technology could end up. DARPA's program was spread over 60 contractors in an effort to ensure total coverage of every possible opportunity.

Today, more than three years later, much of the enthusiasm in the technical and government communities has been lost. Now it is realized that nearly all near term applications address small non-stand alone markets and that large markets are far down stream.

The end result of all of these factors jeopardize the support base, government, industrial, and venture capitalists for the R & D phase of HSTC. Certainly the venture capitalists could not be expected to continue their support unless a dramatic showing by HTSC technology to address large near term markets is realized.

2.2. Goal of HTSC Technology Commercialization Task

The goal of this task has been to identify a significant near term application of HTSC, begin to scope all commercialization requirements needed to be addressed and identify those steps that DARPA needs to undertake so that such applications can be optimally realized for the USA with specific leverage of critical military systems.

2.3. HTSC - MCM

2.3.1. Background

The first application that we have identified is HTSC - MCM. Dr. R.C. Eden is addressing the technical device and system benefits that can be realized from this technology. This is being written in Section 1.0 of this report. Here we discuss the commercialization issues related to HTSC - MCM.

2.3.2. Infrastructure

Fig. 2-1 depicts the needed elements of MCM technology to establish a viable infrastructure. As shown, there is the need to fabricate a multi-layered module as discussed in Sec. 1, low ε substrates, CAE tools, chips that are (perhaps) optimized for low temperature operations, ability to test bare die before mounting them on MCM, ability to have testability on mounted chips to simplify MCM failure testing, the ability to fully test loaded MCM, and cost effective cryogenics. Such an infrastructure does not exist today and must be cultivated if HTSC - MCM is proven to be viable.

2.3.3. Status of Conventional MCM

DARPA - DSO is already funding a conventional MCM program under Dr. Murphy. In this area, it is clear that the merchant infrastructure is weak, while the captive one, which at best could survive at two or three companies, will not be available to other system houses. In this spirit, DARPA is encouraging the MCM development in merchant houses to strengthen this merchant infrastructure and ensure access of this technology to a broad system base. While DSO supports only the MCM fabrication houses, DSO also is monitoring other aspects of the infrastructure to ensure availability of all elements of the MCM technology. Here there exists the embryo of a merchant infrastructure that can be nurtured by government funds. There are at least eight merchant MCM fab-houses and over fifty CAE tools vendors whose products are not complete nor well integrated to satisfy system designers. On the positive side, however, many MCM-houses clearly understand electronics and are able to work with system houses to ensure proper development of insertable MCM technologies.

2.3.4. Status of HTSC - MCM

Most players in HTSC technology, on the other hand, are materials engineers and scientists and most of these are ceramicists having had little or no experience as to what an MCM is, let alone testing, CAE tools utilities, system needs, customers, markets, etc.

Obviously, if HTSC - MCM infrastructure is to be realized the make-up of HTSC community involved in this area has to be infused with significant electronic know-how.

The HTSC community not only must establish a technology that is compatible with the silicon industry, but must also be in position to dialogue and market to system houses directly. If the discussions in the first section of this report do materialize, indeed a total system could be integrated on a 8" x 8" card. Today none of the current HTSC merchant houses are in a position to address this market.

2.3.5. Activities During the Last Three Months

We have held several meetings and have had numerous discussions with STI, Conductus, Encore, MIT, Cornell, Georgia Tech, Stanford, Berkeley, National Labs, several divisions of E-Systems, semiconductor houses, Cray, DEC, and MCC all in an effort to define a road way that could lead to a merchant HTSC - MCM product recognizing where the HTSC technology and the community are at. We have received strong support and enthusiasm from the community for the establishment of an HTSC - MCM program. The recognition to focus our resources has been quite strong. Towards that end, we have proposed a program, depicted in Fig. 2-2, to be sponsored by DARPA, which we feel could meet the goals stated in Section 2.1. It is felt that if we can succeed in developing a cost effective HTSC - MCM technology, indeed the market will be large and near term 5 - 7 years. This we feel could excite the technologist, the system houses and the financial and business communities.

From a macroscopic point of view, the program will consist of two phases. Phase 1 is an R & D phase designed to demonstrate (1) proof of concept of an HTSC - MCM manufacturable process, (2) HTSC - MCM benefit at the system and device level, and (3) establish a process for infusing electronic know-how to the HTSC community.

Phase 2 will consist mainly of manufacturing technology development and the establishment of a viable merchant HTSC - MCM infrastructure.

In Phase 1, the players will include for the first MCM team Cornell, led by R. Buhrman, MIT, led by M. Cima; Georgia Tech, led by P. Kohl; E-Systems, led by D. Kraussman of Melpar; and K. Seawright of Greenville Divisions respectively; STI, led by R. Hammond; Conductus, led by J. Rowell. Since E-Systems is a systems house heavily involved in DOD programs that require high electronic system performance and have had intimate relationships with the conventional MCM infrastructure and high performance computer industry, we propose that they lead the total effort as shown in Fig. 2-3.

Other players who should be added to the second phase are companies like Cray and CAE Tools teams. It is recommended, that for the time being, Quad continue to be funded independently to help address the CAE tools technology and services to additional MCM teams that may be formed later on.

Initial milestones for the recommended team will be definitized in a meeting to be convened for all players in January 1991. Many meetings have taken place with the E-Systems engineering to define the process and methodology of implementing this HTSC - MCM program, and for ensuring that the technical and commercialization milestones can be achieved in a cost effective manner. E-Systems has had significant experience in such MCM programs.

During the next quarter, we plan to study the possibilities of initiating other programs similar to the one headed by E-Systems.

2.3.6. Program Emphasis

Since all that has been demonstrated to this point has been limited to paper studies, and since it is clear to all potential participants that the difficult challenges of demonstrating proof of concept at several levels, technical, manufacturing, and marketing, still lie ahead, it is prudent that the resources in the industrial community be wisely deployed to address the R & D issues collectively. This means the program in spirit should emphasize that the R & D community work together and that the successful technologies be transferred to all vendors interested in the commercialization aspects. To this end, efforts are taken to assemble the teams that recognize that the major goal of Phase 1 should be the validation of the technology and its successful smooth transition to industry. For this reason, students and professors in universities will be encouraged to spend significant time in industry while the program is actively in progress.

The effect of those activities would be to produce students who not only know HTSC processing, but also who understand MCM technology. This should be extremely beneficial to the merchant HTSC vendors who also need to grow an in-depth MCM know-how at all levels and have in effect no sources to hire engineers who understand HTSC technology, MCM technology, and electronic system requirements. In the meantime HTSC houses by interacting directly with system houses and with MCM engineers at Georgia Tech and MCM engineers at E-Systems will in time evolve the internal talent required to address the MCM technology and market. E-Systems which has strong internal MCM application programs and strong ties to conventional MCM houses will serve to guide the development of HTSC - MCM technology and at the same time introduce the HTSC houses to commercial and defense market segments.

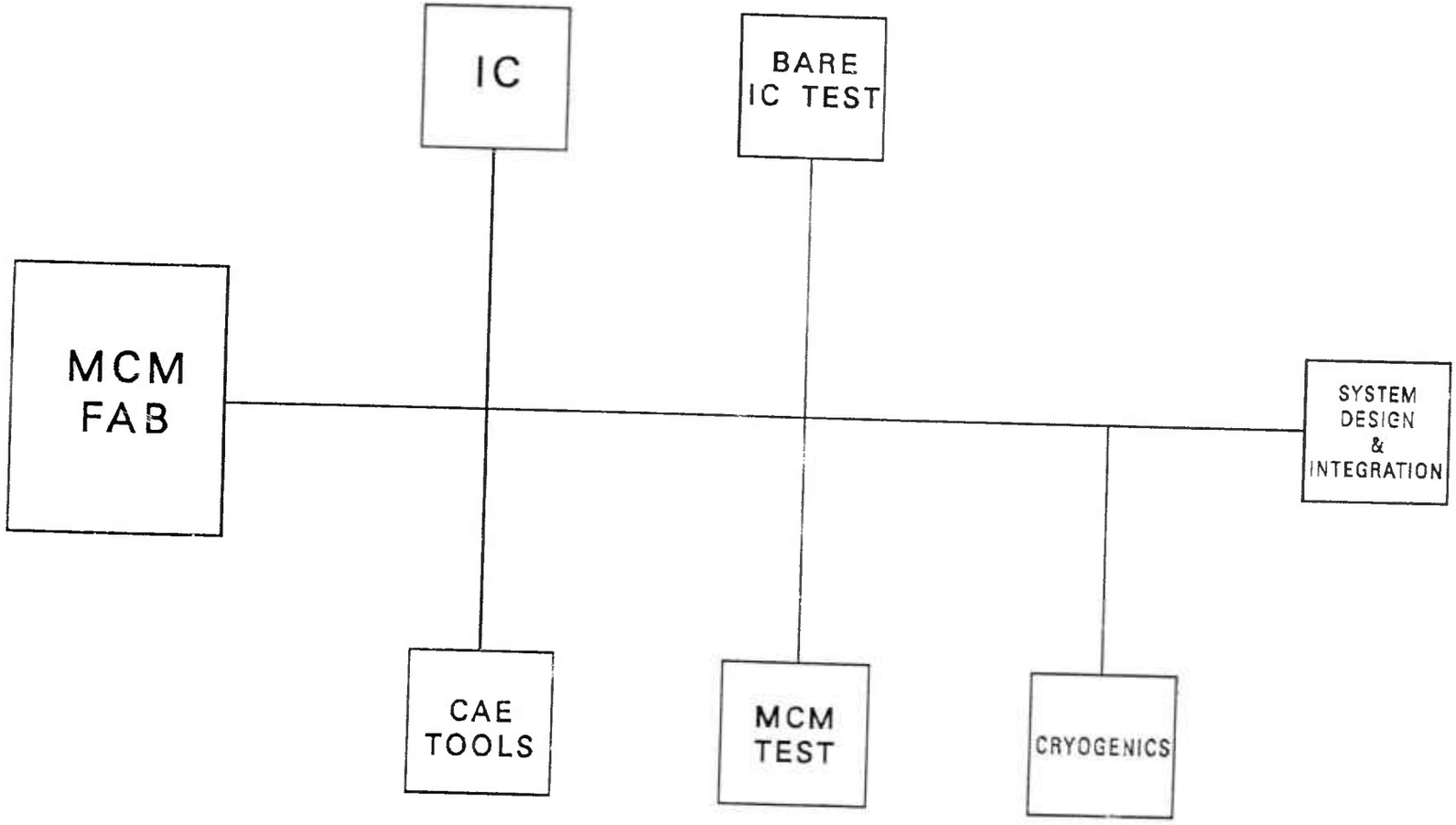


FIG. 2-1: MCM INFRASTRUCTURE

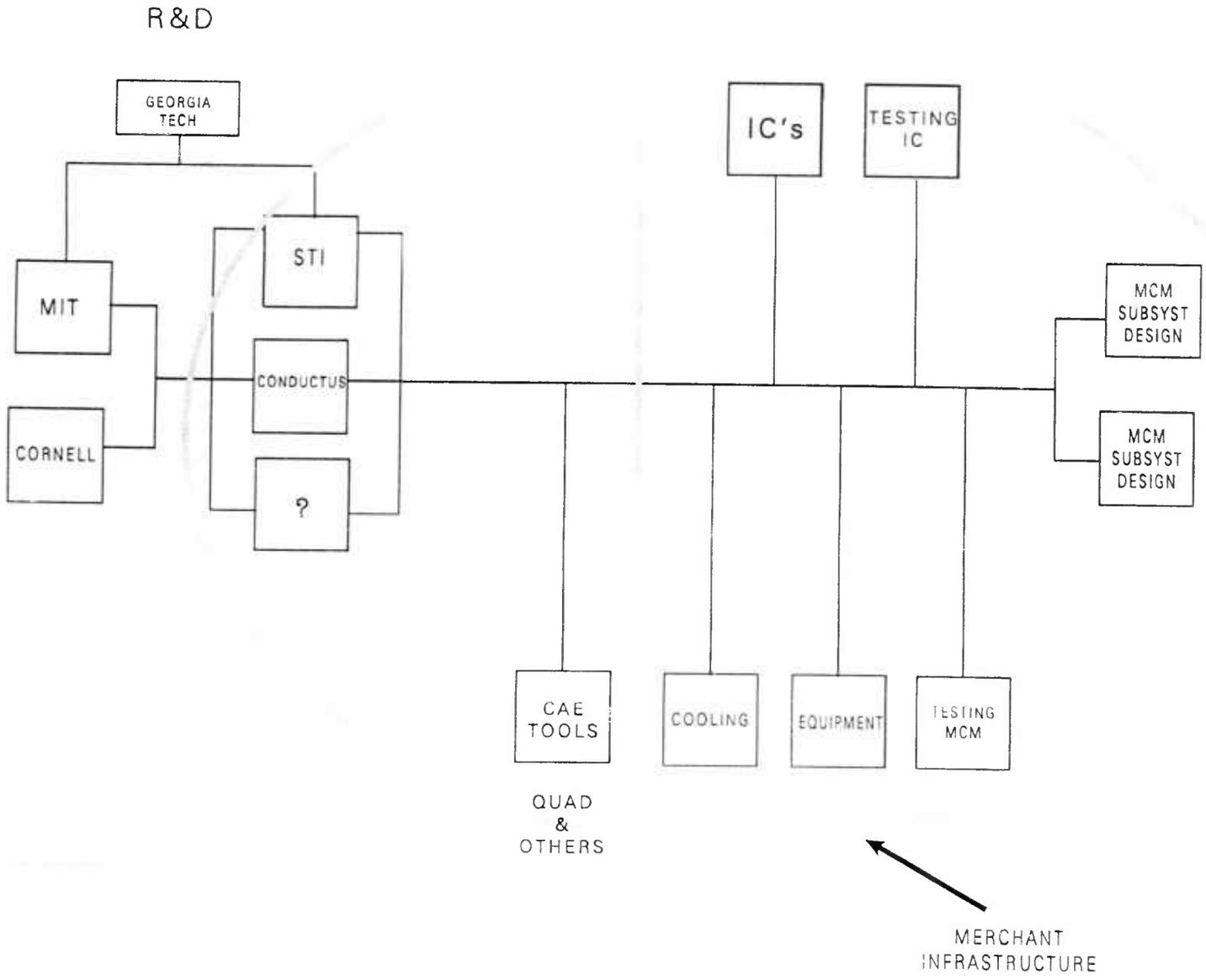


FIG. 2-2: R & D AND PRODUCT DEVELOPMENT PHASES

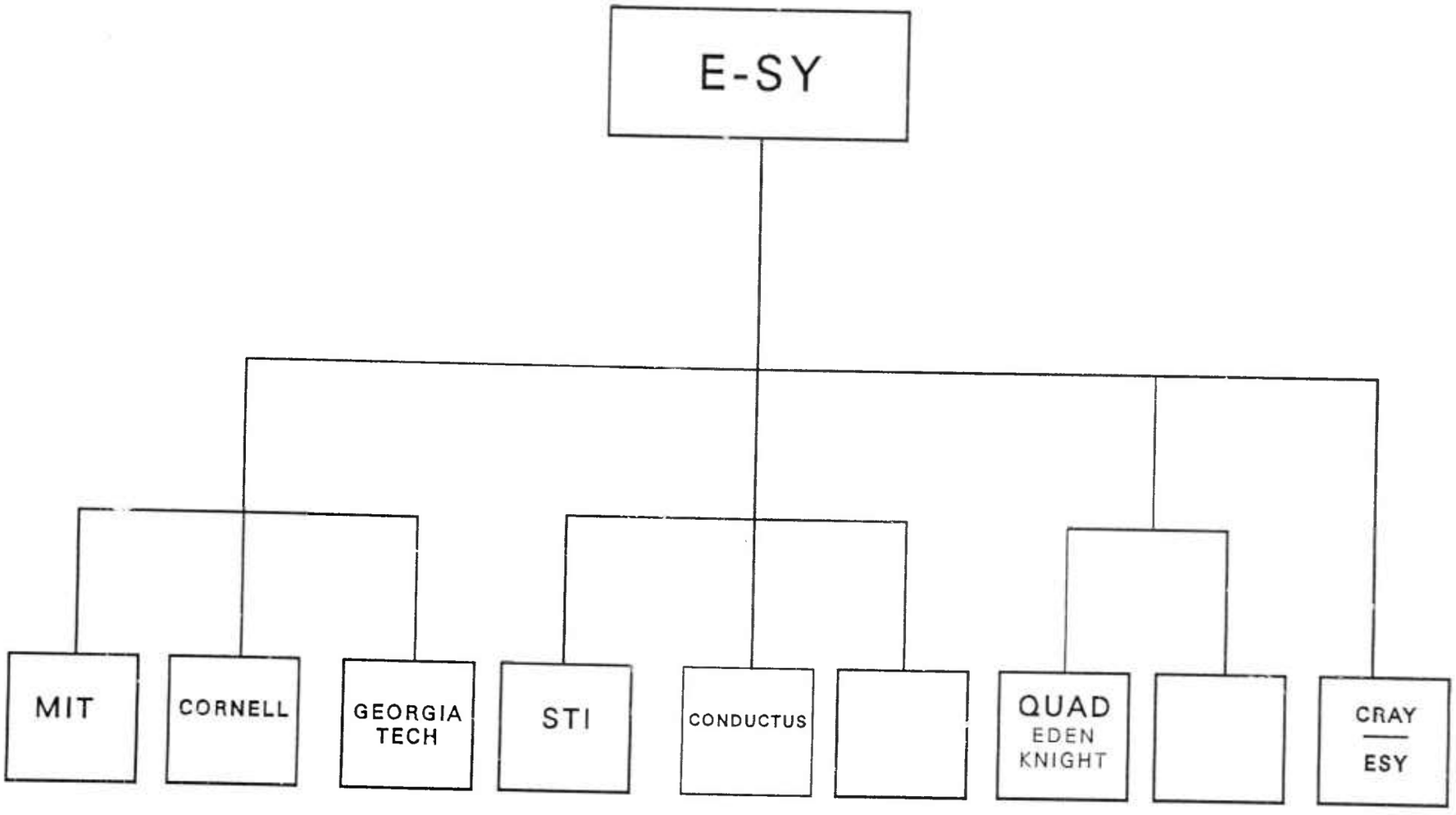


FIG. 2-3: PROGRAM ORGANIZATION

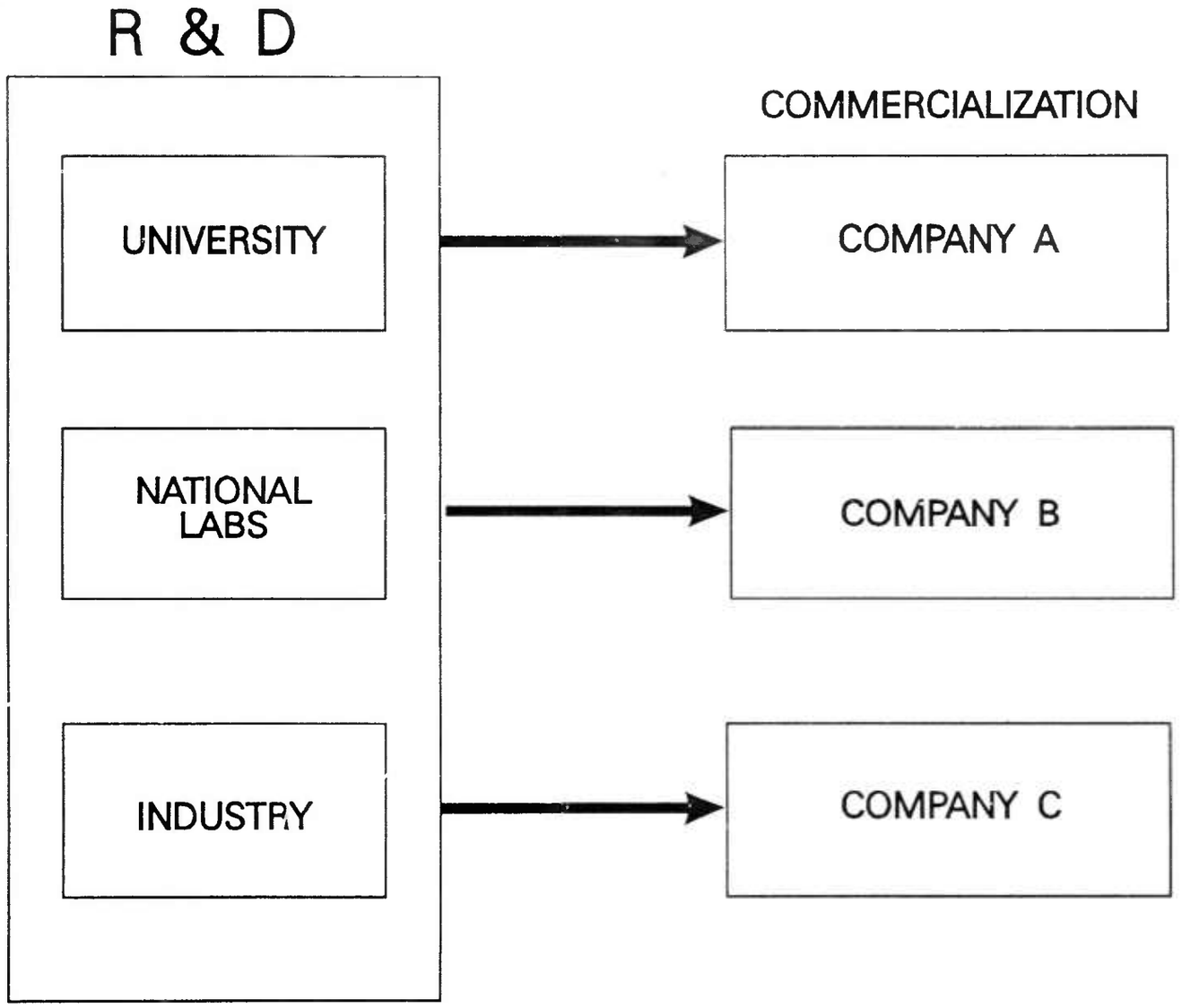

R & D
UNIVERSITY
NATIONAL LABS
INDUSTRY
COMMERCIALIZATION
COMPANY A
COMPANY B
COMPANY C

FIGURE 2.4

3.2 Q1 1991 Quarterly Report

Section 1.
Technology Requirements

Magnetic Flux Density Calculations

In response to comments by Professor Malcolm Beasley of Stanford (initial concerns related to Dr. Frank Patton, with follow-up phone conversation and visit by R. Eden to Stanford) concerning flux penetration into HTSC lines, (with consequent high frequency signal loss) if the B-field exceeds 100 Gauss or so on good HTSC material, analysis of the expected flux densities for MCM applications has been carried out. Of particular interest is the importance of (if any) the HTSC line thickness as well as linewidth and ground configuration (eg. microstrip or stripline).

Analytically, one can use basic magnetic field principles ($B = uH$, where $uo = 4\pi \times 10^{-7}$ Webers meter-ampere, and $\oint H \times ds = I$ the closed loop integral of H equals the enclosed current) to obtain the magnetic field strength at the surface of a number of configurations. For example, for a circular conductor of diameter, d (in meters), the path length at the surface (the circumference) is πd, so $Havg = I/\pi d$, or (using 10 Gauss = 1 Tesla = 1 Weber/meter^2), we have

$$Bavg\ (Gauss) = \frac{4 \times 10^{-3}}{d\ (meters)}\ I\ (amperes) \quad \text{Circular Conductor} \qquad (1)$$

For example, for d = 2um (2×10^{-6} meters) and I = 20mA, we have B = 40 Gauss at the surface of the circular conductor (assuming radial symmetry as in a coax cable).

In a symmetrical stripline configuration with a very wide conductor width (W>>h, t where W is the conductor width, t its thickness and h the separation from the ground planes), the return currents in the ground planes cancel at the signal conductor and so we have $H = I/2W$, or

$$B\ (Gauss) = \frac{2\pi \times 10^{-3}}{W\ (meters)}\ I\ (amperes) \quad \text{Wide Stripline} \qquad (2)$$

where as always, we are assuming u = uo (non-magnetic dielectric). for this symmetrical stripline case, with W = 2um and I = 20mA, we get B = 62.832 Gauss.

For the case of micostrip, where there is only one ground plane, the return current in the ground plane generates a magnetic field which adds to that of the signal line in the space between the two, so that we have H = I/W (again, for very wide lines), and hence,

$$B\ (\text{Gauss}) = \frac{4\pi \times 10^{-3}}{W\ (\text{meters})}\ I\ (\text{amperes})$$ Wide Microstrip Eq. 3.

Here, for the same I = 20mA, W = 2um case, we have B = 125.664 Gauss, which potentially gets us into the problem region where magnetic flux could drive into even pretty good HTSC materials.

We note that these simple case estimates vary by a factor of π for these different configurations. The factor of $\pi/2$ between the circular conductor and the flat, wide symmetrical stripline is simply due to the fact that a circular conductor has a factor of $\pi/2$ larger periphery than a flat conductor, and the additional factor of 2 due to the fact that in wide microstrip the current flows only on one side of the conductor. In the real HTSC MCM application, the signal interconnect transmission lines will not be wide striplines or wide microstrip (the impedance would be too low), but rather reasonably narrow line microstrip or stripline-like configuration. We need to have an idea of the magnetic field strengths in such practical HTSC configurations, with linewidths of the order of 1.5um to 2um and geometries (eg. dielectric thicknesses) such as to give line impedances near 50 Ω with reasonable dielectric constants (ϵ_r = 3.9 taken in these calculations). The effect of the narrow linewidths is to make fringing very important, so that a full 2-d Laplace equation analysis is required. Note that if we assume rectangular cross-section conductors, there is a singularity at each corner, at which the B-field becomes infinite (assuming perfect conductor conductivity), so that at these sharp corners the HTSC material will tend to go normal, in effect "rounding" the corners. Hence, field simulations were done with both "sharp-cornered" and rounded corner conductors for comparison.

Figure 1 shows half of the 8 geometries analyzed (the other 4 are identical except that the thickness of the signal line is reduced to t = 0.1um instead of t = 0.75um in Figure 1). All conductors have W = 1.5um, spaced from the ground plane(s) W, h = 1.25um for the microstrip (right hand side of Fig. 1) cases and h1 = h2 = 2.0um for the symmetrical stripline cases at the left. The corner radii arbitrarily chosen for the t = 0.75um conductors was 0.325um (which corresponds to an 8.06% reduction in area compared to the

1.5um x 0.75um rectangular "square-cornered" conductor). For the thin (t = 0.10um) rounded conductors, a radius of 0.05um was assumed. The filename identifiers in Fig. 1 are those used in the other figures in this report for reference.

Fig. 2 shows magnetic flux lines for the rounded microstrip case shown at the lower right in Fig. 1. The surface magnetic field strength is indicated by how near the closest flux line spaces to the conductor surface. In a wide microstrip, the flux lines would be equally spaced between the ground plane and conductor. But here they are closer at the conductor, particularly near the "corners". This is particularly noticeable for the square-cornered microstrip case of Fig. 3 where the first flux line comes very near the corner. For the very thin (t = 0.1um) case of Fig. 4, the field concentration is greatest near the conductor edge. Note that only half of the conductors are shown in Fig's. 2-4, since the fields are equal on the other half by symmetry.

These flux line plots can themselves be used to get a reasonable quantitative measure of the magnetic field strength at the surface (which) is proportional to the surface current density on the conductor). While the Quad Design Systems tools have this information available directly (and are used to calculate conductor skin effect losses, for example), the results shown in Fig's. 5-9 were in fact obtained through graphical analysis of the flux plots and hence are not nearly as accurate, but are quite adequate for our purposes here.

Figure 5 shows the effect of the square corners in a symmetrical stripline configuration (left side of Fig. 1) by comparing the rectangular conductor to the rounded case. Plotted is the magnetic flux density or B-field, in Gauss, as a function of position from the top center of the conductor to the right edge, generated by a 2.0mA current through the 1.5um x 0.75um conductor. The field, about 50 Gauss at the edge, builds to about 80 Gauss at the corner for the rounded conductor, or nearly twice this for sharp corners (actually infinite, of course, but the graphical method used averages somewhat, simulating a small degree of rounding).

Fig. 6 compares the rounded and square-cornered cases for microstrip lines, again with the I = 20ma current level and 1.5um x 0.7um line sizes. At the left is the field on the ground plane side center of the conductor, moving around the conductor to the opposite side (it is further around the square-cornered conductor than the rounded case so the two curves do not stop at the same point. The normalization of all the curves was verified by checking that the integral of B/uo equals the conductor current (so the areas of these curves are equal). Note that for a wide microstrip, the field would be essentially zero to the right of

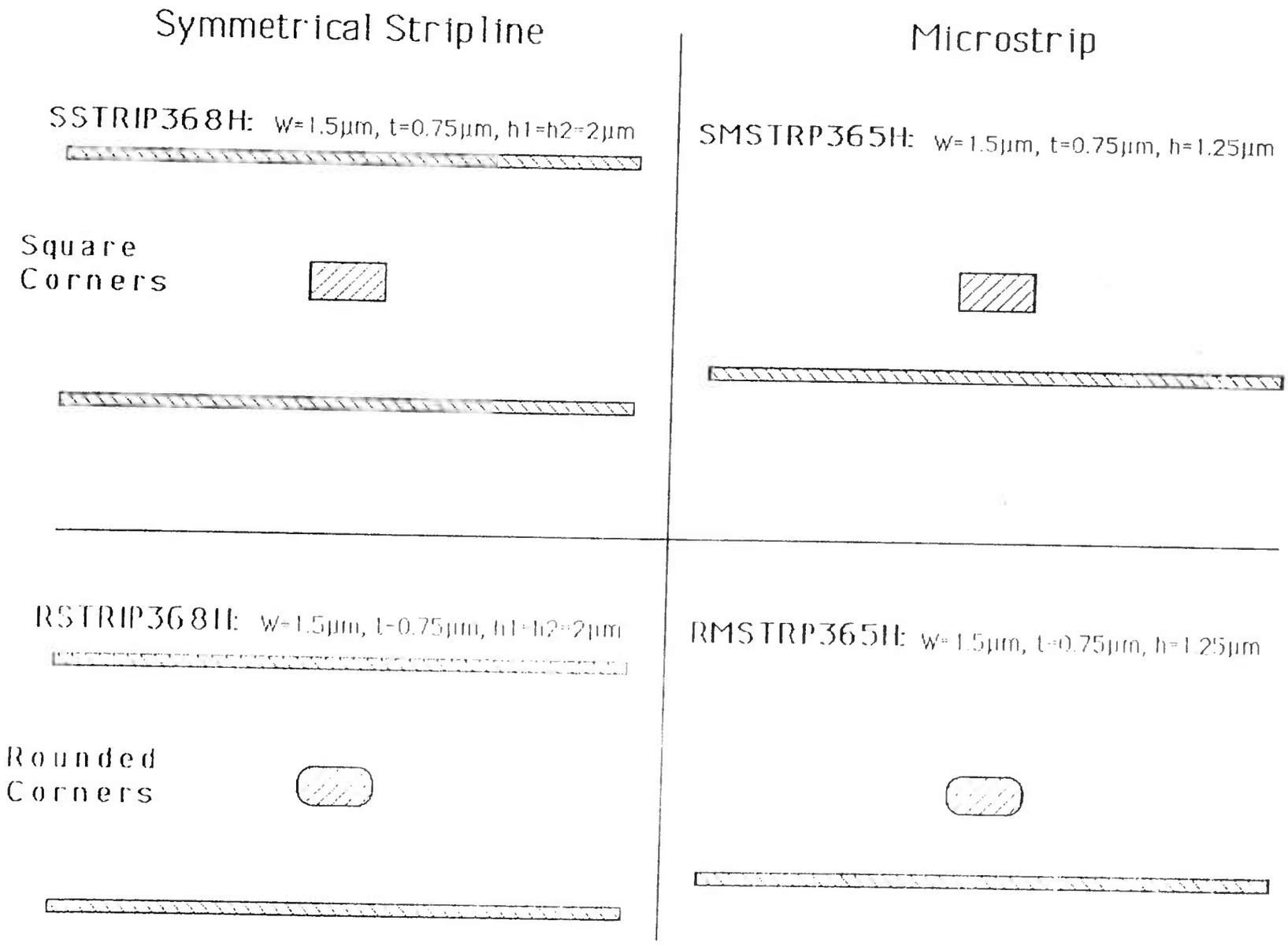


Figure 1. HTSC Interconnect Transmission Line Configurations analyzed. Both thick (t = 0.75um) and thin (t = 0.10um) signal conductor layer thicknesses were analyzed using the same conductor to ground plane spacings (h) as shown here.

]FIGURE_2.plt

Config: FIGURE_2

Conductor: 1

Mode: MAGNETIC

x_range -4.88 5.62

y_range 0.20 3.65

RMSTRP365H: W=1.5um,
t=0.75um, h=1.25um

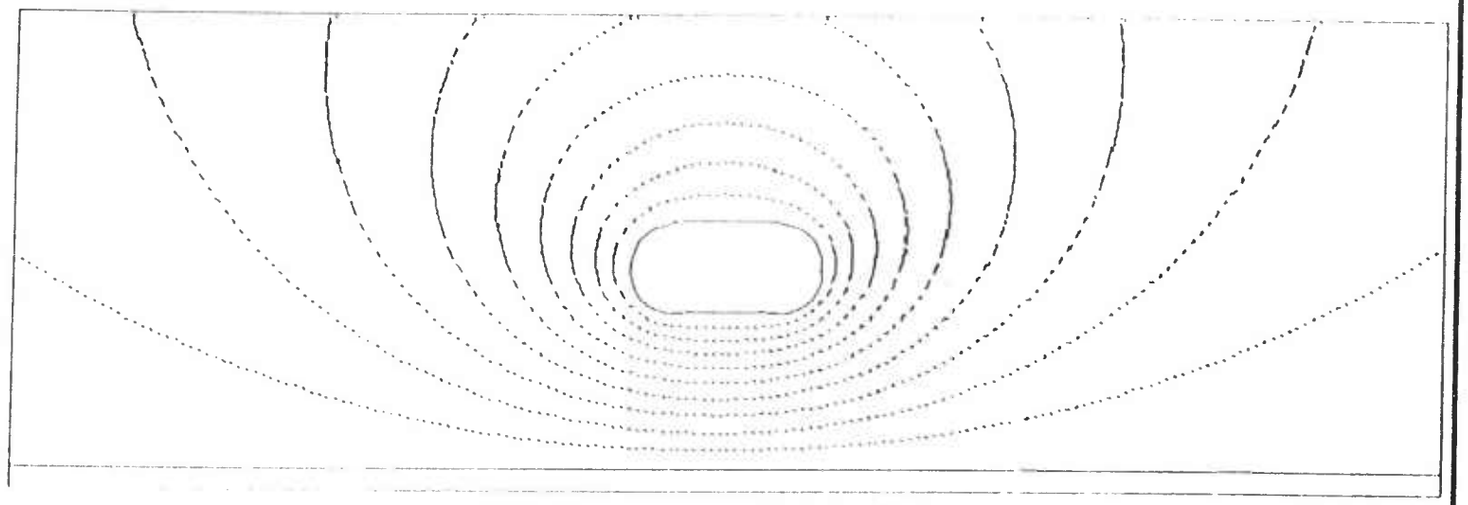


Figure 2. Magnetic flux lines for microstrip with thick rounded-corner conductor. Result obtained by Quad Design Technology's XFX, Crosstalk Field Extractor.

IFIGURE_3.plt

Config: FIGURE_3

Conductor: 1

Mode: MAGNETIC

x_range -4.88 6.38

y_range -0.20 3.65

SMSTRP365H: W=1.5um,
t=0.75um, h=1.25um

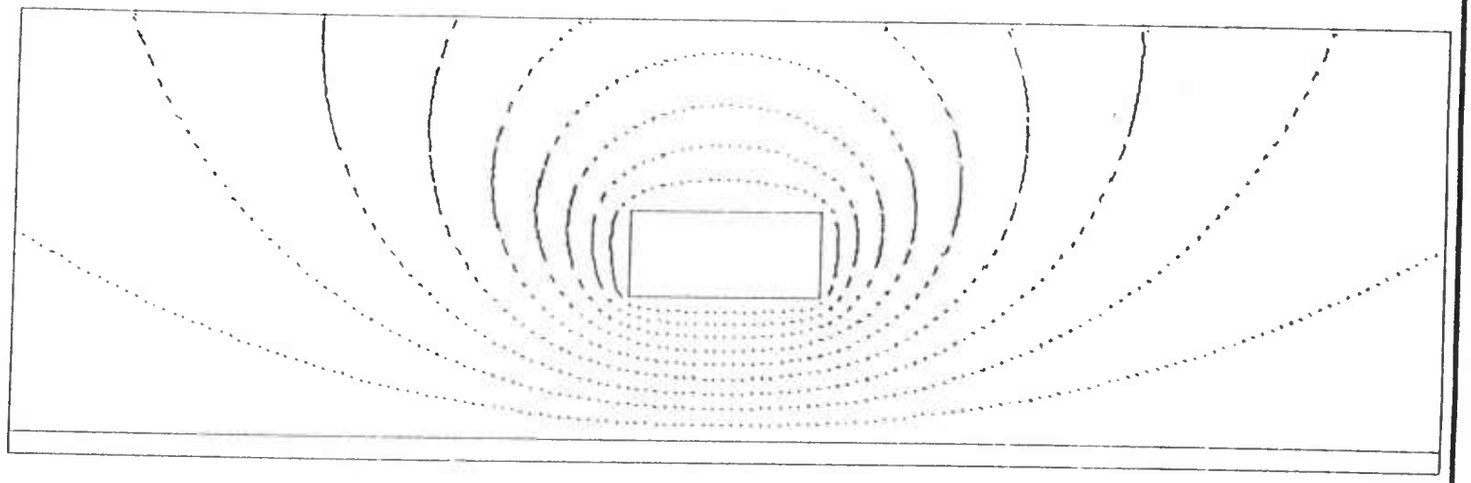


Figure 3. Magnetic flux lines for microstrip with thick rectangular (square-cornered) conductor. Result obtained by Quad Design Technology's XFX, Crosstalk Field Extractor.

Figure 4. Magnetic flux lines for microstrip with thin, rounded-corner conductor. Result obtained by Quad Design Technology's XFX, Crosstalk Field Extractor.

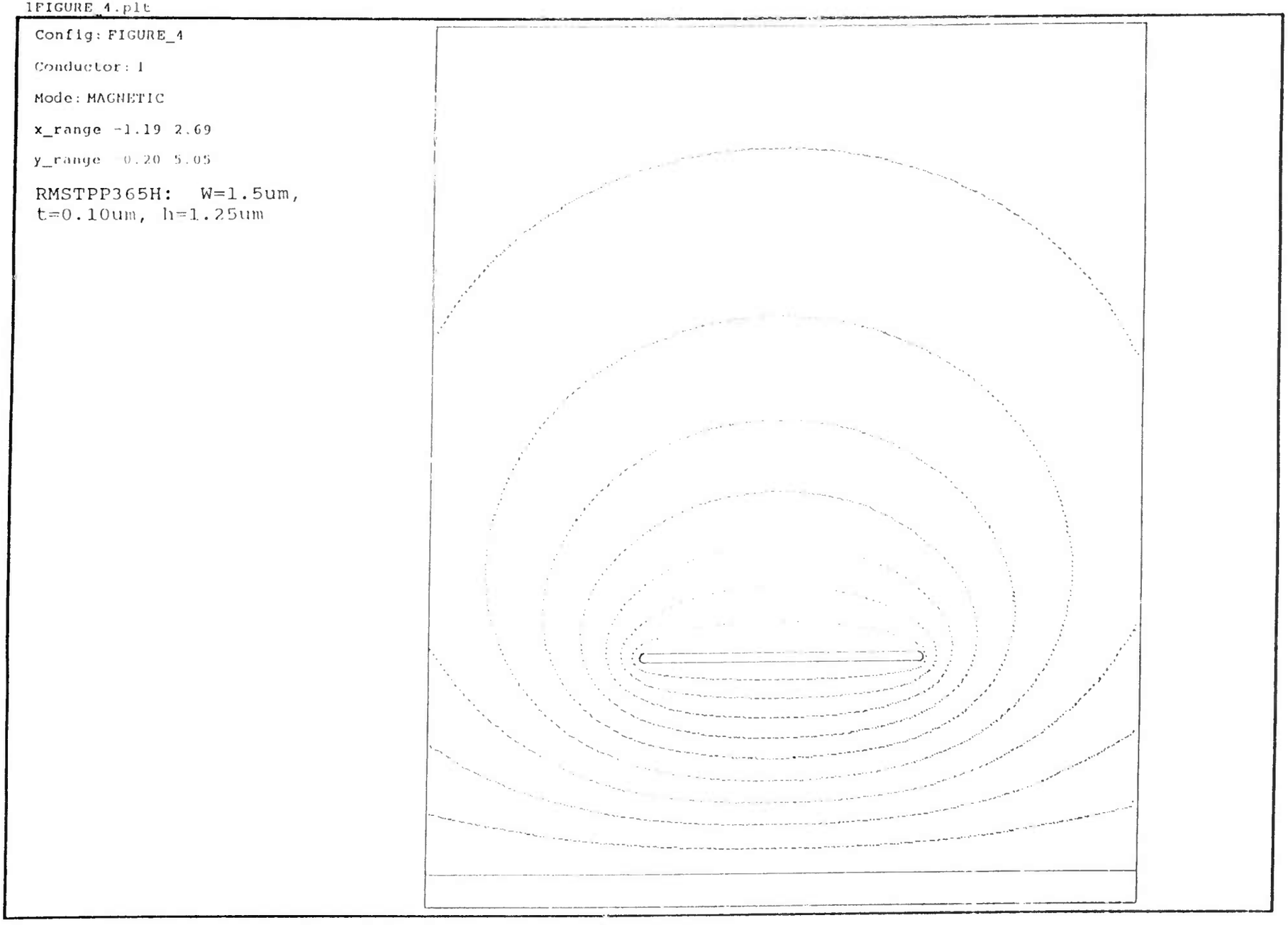
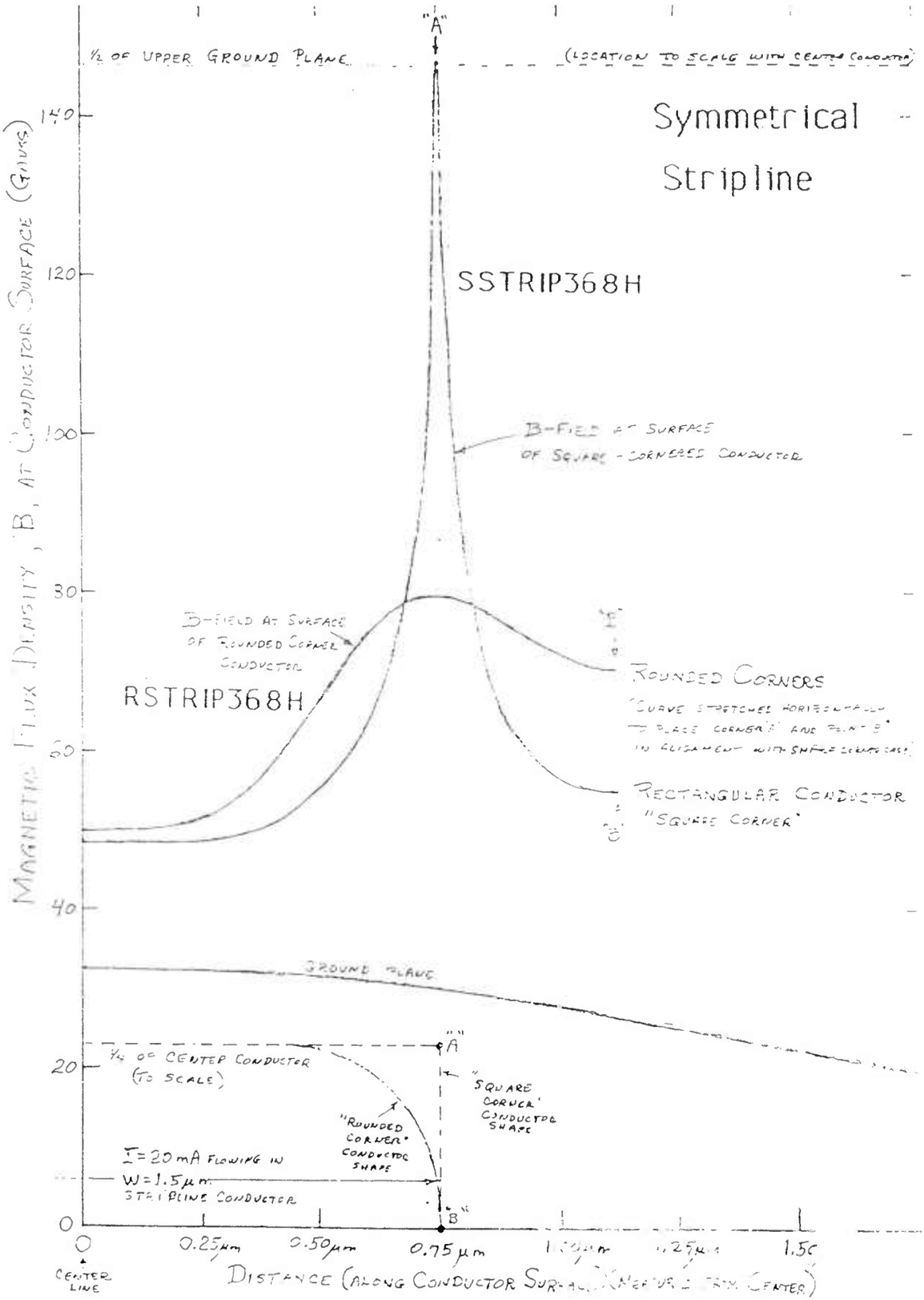


Figure 5. Comparison of B-field at the surface of rounded and square-cornered HTSC conductors in a symmetrical stripline configuration (I = 20mA flowing in 0.75um x 1.5um conductor).



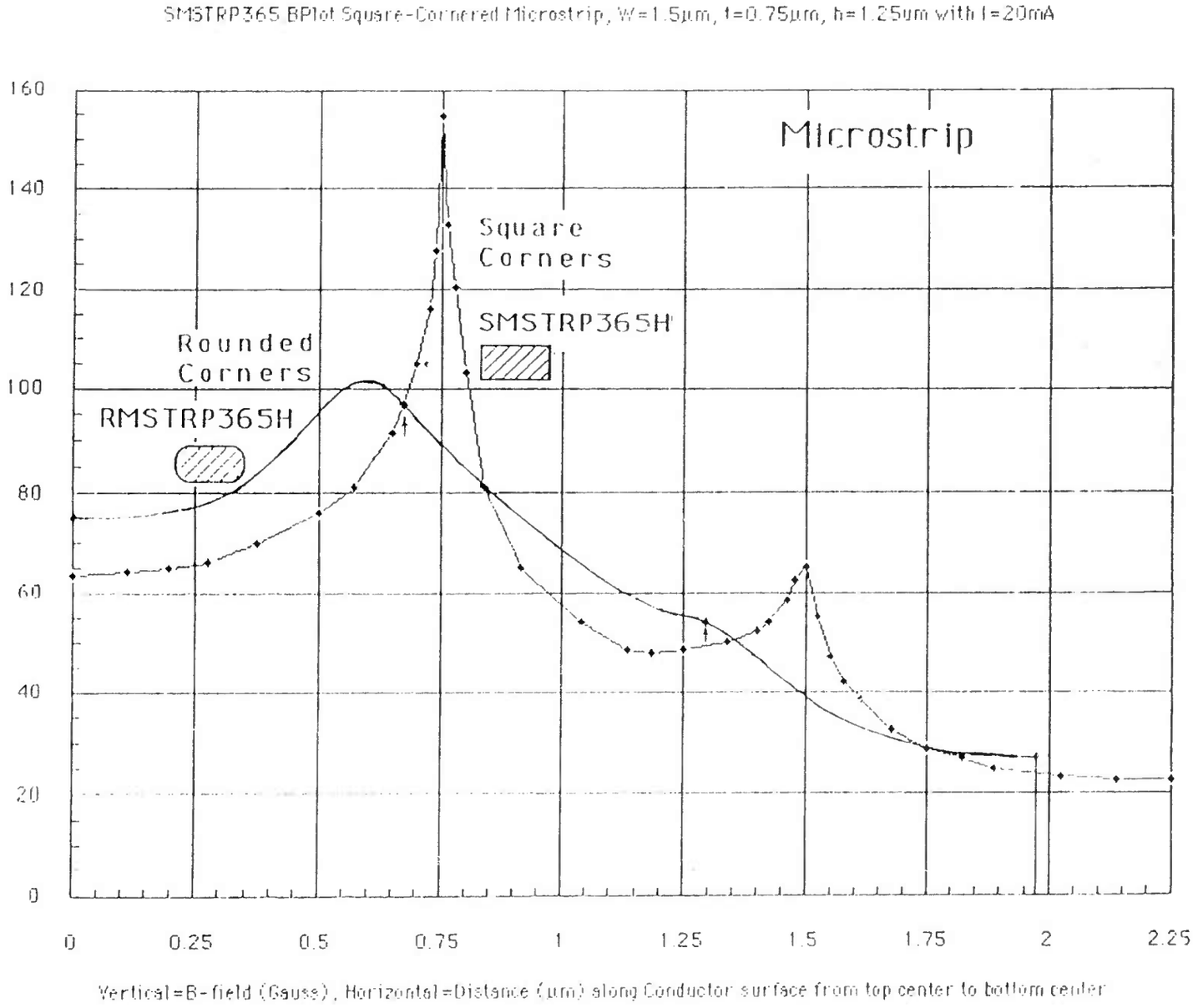


Figure 6. Comparison of B-field at signal conductor surface for microstrip with square-corner and rounded conductors.

center (backside of conductor), but for reasonably narrow lines as shown here, the B-field at the back center is about 37% of that at the center of the ground plane side. This means that overcoating the HTSC lines with a thick lossy normal metal could cause very serious line losses.

While Eg. 3 predicts for wide microstrip a 2x higher B-field than wide stripline (Eq. 2) in fact the difference is not nearly that large. This is quite clear in Fig. 7 which compares the rounded conductor microstrip and symmetrical stripline cases for 1.5um x 0.75um conductors. At the groundside center of the microstrip, the B-field (75 Gauss) is 50% higher than for symmetrical stripline (50 Gauss). The peak "corner" field, 100 Gauss for the microstrip is only about 30% higher than that for the stripline, and the edge field is identical ($\sim$70 Gauss).

When the conductors get very thin, however, this edge field gets very large, as illustrated for the stripline case in Fig. 8. Here, for the roundest t = 0.1um conductor thickness case, the edge B-field (right side of the curve) hits nearly 200 Gauss, compared with a peak corner field of under 80 Gauss for the t = 0.75um rounded conductor case. In fact, for such a thin conductor, there is very little difference in peak field strength for the microstrip and symmetrical stripline cases shown in Fig. 9 (both nearly 200 Gauss for this I = 20mA, W = 1.5um, t = 0.1um condition). If it is indeed the case that B-fields above 100 Gauss or so may cause flux-penetration losses even in fairly good quality HTSC films, then the use of very thin (0.1um = 1000 Å) films for HTSC conductors may be precluded.

Conclusion from B-Field Analysis

In addition to the observations made above, a few general conclusions may be drawn.

1. The concern that the surface B-fields in small HTSC MCM signal lines (eg. 1.5um to 2um or so) would be so high as to render them quite lossy at high frequencies does not appear to be justified as long as reasonable conductor geometries are used.

2. The corner singularity of B-field at sharp conductor corners may render a small volume of HTSC material normal under high current conditions, leading to nonlinear, frequency dependent losses, harmonic generation, etc. (things which could be quite serious in linear analog applications, but are not very significant in digital systems). However, as long as the HTSC conductor layers are quite thick, as the extreme corners go normal, the conductor edges are effectively rounded which sharply drops the peak fields

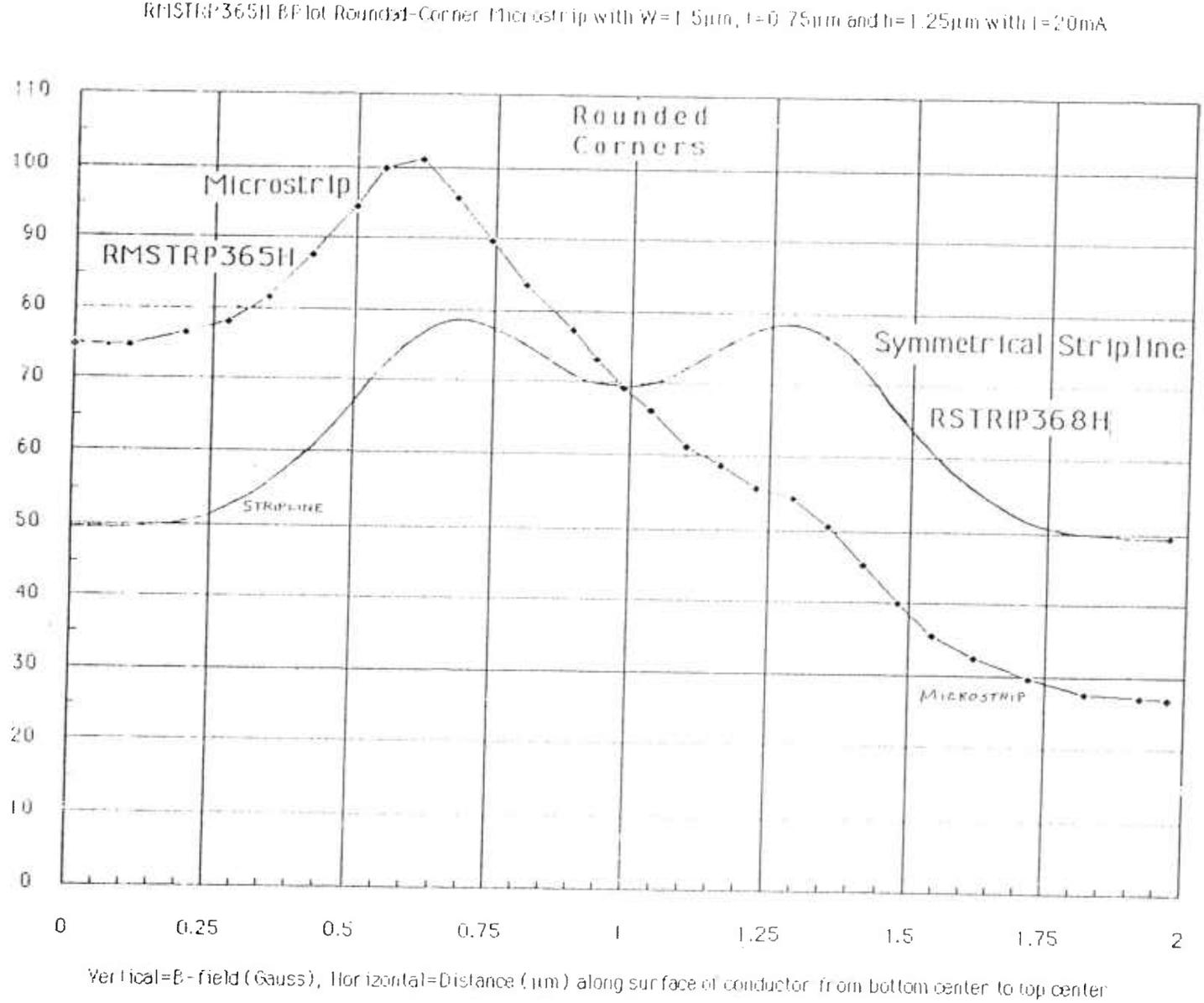


Figure 7. Comparison of magnetic field strength for microstrip line with that for symmetrical stripline for identical 0.75um x 1.5um rounded conductor shape.

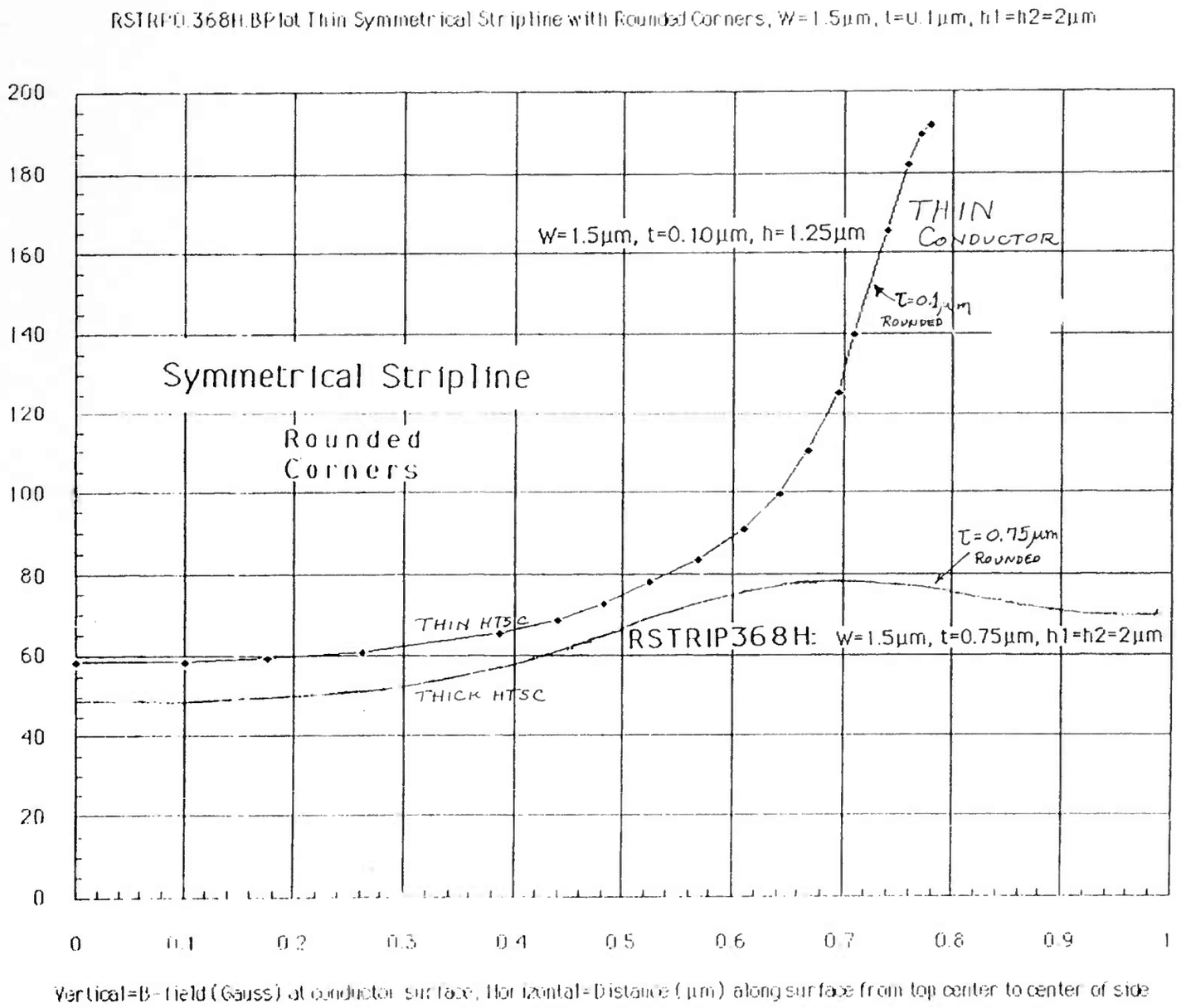


Figure 8. Comparison of magnetic field strength for thick (t = 0.75um, W = 1.5um) rounded corner HTSC conductors in the same symmetrical stripline configuration. Note high edge fields for thin case.

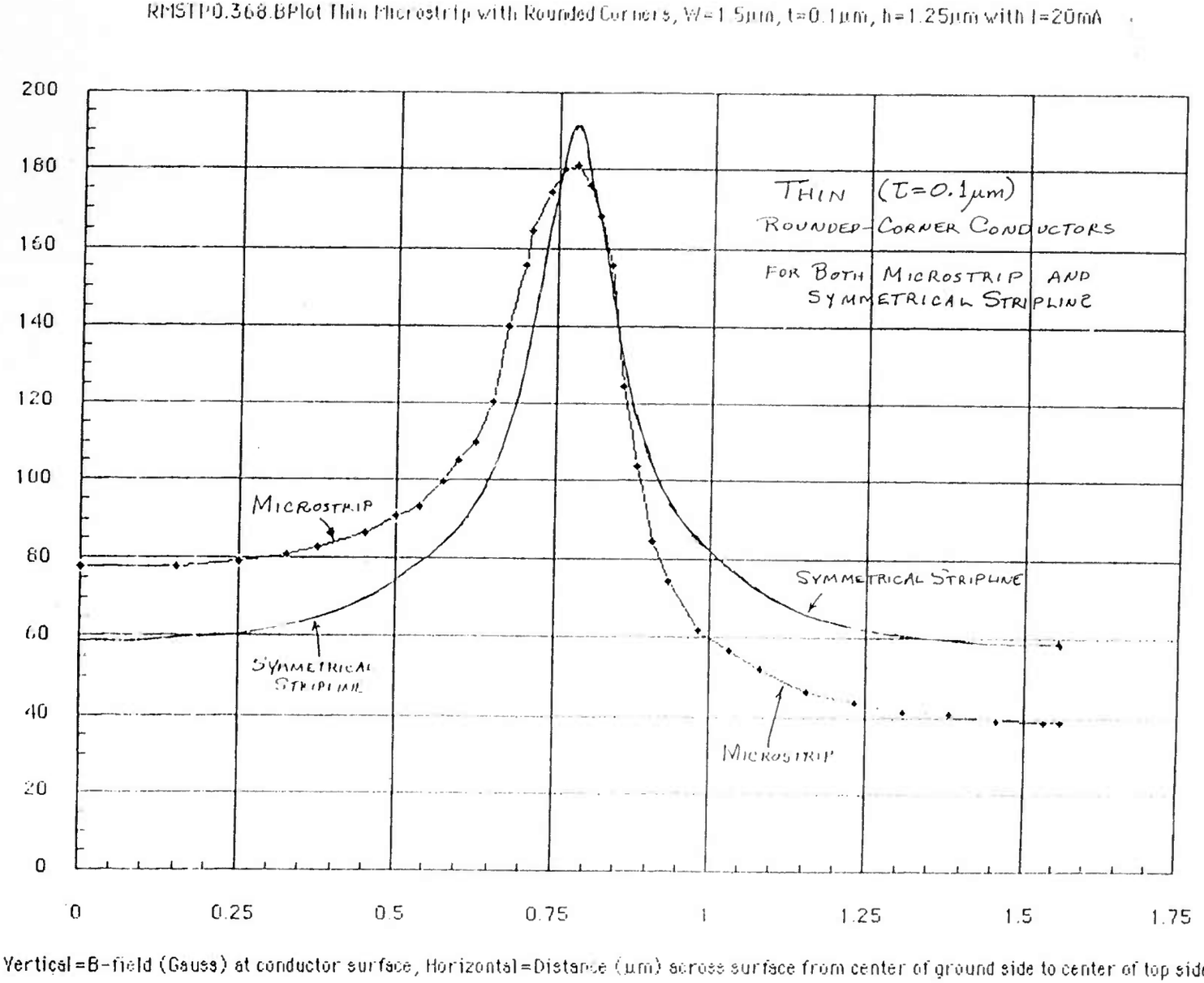


Figure 9. Comparison of B-fields for microstrip and symmetrical stripline configurations for thin (t = 0.10um, W = 1.5um), rounded-corner HTSC lines. Unlike thick conductor case of Figure 7, peak B-fields (at edge) are similar for both.

so that only very small volumes of material are affected, and the attendant losses should be very small. (Keep in mind that 5% to 10% losses of pulse leading edge height are generally acceptable in digital systems without serious degradation of noise margin or performance).

3. If the HTSC conductor layers are too thin (eg. 0.1um), the high concentration of B-field at the edges (even if they are radiused) could lead to significant loss problems unless the threshold for flux penetration can be pushed above 200 Gauss. The safest course might be to use fairly thick HTSC layers (eg. 0.5um), which also might help with defect problems (a thick normal region near the defect could still handle the current with low resistance). Of course, it is sometimes difficult to maintain proper orientation in thick growths of HTSC's, so that could be a relevant technology concern as well. These issues will, of course, be resolved experimentally, using pulsed line loss measurements on fineline structures.

4. The peak B-fields at the ground planes (see Fig. 5 for example) are about 32 Gauss for the symmetrical stripline and about twice this for microstrip. Hence, reasonable quality HTSC materials are required for the ground planes as the current densities are still quite high.

5. There is not an enormous difference in B-field at the conductor between the symmetrical stripline and microstrip cases (nowhere near the 2x predicted for wide lines in Eq's. 2 and 3). With proper design, either should be workable in the HTSC MCM environment, as would other line configurations (eg. triplate, coplanar, hybrid coplanar/microstrip, etc.), given proper design.

6. There is still a lot of B-field and current density on the back side of narrow microstrip lines so that coating with normal metals, if they are very thick (eg. comparable to their skin depth), will give a lot of high frequency loss.

In summary, this exercise has given a lot of useful design guidance, but first and foremost, the applicability of HTSC interconnects for high density MCM's still looks excellent.

Internal Inductance and Loss

Two key advantages that HTSC interconnect structures would have are the related properties of lower skin resistance and lower internal inductance. The latter effect can be particularly important for signal propagation when one considers the thin metal used in MCM's. In the last quarter, a model was developed for both normal metal microstrip and stripline skin effect losses and internal inductances, and the results compared against measurements taken from sample MCM structures with the results being generally in excellent correspondence with measurements (see Table 1 and Table 2). The models that were used were:

$$L(f) = L_{ext} + (1/\sqrt{2\pi f}) \times K_s \times G(f)$$

$$R(f) = R_o + (\sqrt{2\pi f}) \times K_s \times G(f)$$

where:

L(f) = Total Inductance per unit length
R(f) = Total Resistance per unit length
Lext = External inductance per unit length (perfect conductor)
Ro = DC Resistance
Ks = Coefficient of Skin resistance

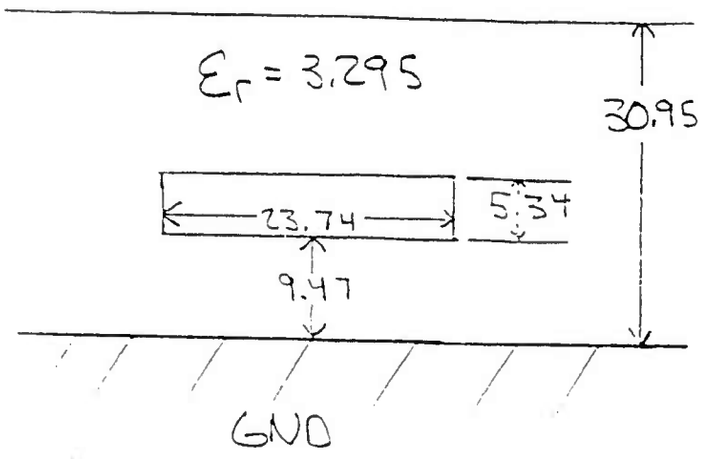
$$G(f) = \frac{1}{2}\left[1 + \frac{\sinh(2t') - \sin(2t')}{\cosh(2t') - \cos(2t')}\right] \text{ for stripline}$$

$$= \frac{1}{2}\left[1 + \frac{\sinh(t') - \sin(t')}{\cosh(t') - \cos(t')}\right] \text{ for microstrip}$$

$t' = t/\delta(f)$
t = Metal fluckness
$\delta(f)$ = Skin Depth

Note as $f \to \infty$ $G(f) \to 1$. CAE field extraction tools such as Quad Design's XFX can calculate the Ks *Lext* & Ro coefficients and so the total resistance and inductance can be computed.

CONFIGURATION MICROSTRIP

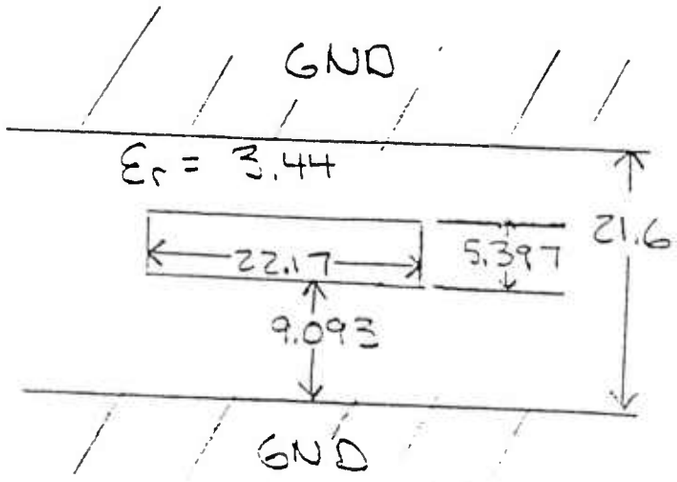


Capacitance = 3.809 pF

freq MHz	Ltotal nH	Zt(G) ohms	skin depth microns	MEASURED Inductance nH	%diff Ltotal & MEASURED
5	16.19	65.19	36.41	16.2	-0.09
21	11.41	54.72	17.77	11.5	-0.80
41	10.11	51.52	12.72	10.0	1.11
61	9.52	50.00	10.42	9.39	1.41
81	9.17	49.06	9.05	9.03	1.53
101	8.92	48.40	8.10	8.77	1.75
121	8.74	47.91	7.40	8.60	1.6
141	8.60	47.52	6.86	8.47	1.54
161	8.48	47.20	6.42	8.40	1.01
181	8.39	46.93	6.05	8.35	0.46
201	8.31	46.70	5.74	8.33	-0.29

Table 1. Theoretical versus measured internal inductance for microstrip MCM geometry.

CONFIGURATION STRIPLINE



Capacitance = 6.604 pF

freq MHz	Ltotal nH	Zt(G) ohms	skin depth microns	MEASURED Inductance nH	%diff Ltotal & MEASURED
5	13.68	45.51	36.41	14.1	-2.98
21	8.83	36.56	17.77	9.33	-5.37
41	7.51	33.73	12.72	7.81	-3.78
61	6.92	32.37	10.42	7.15	-3.24
81	6.56	31.52	9.05	6.75	-2.81
101	6.31	30.92	8.10	6.46	-2.26
121	6.13	30.47	7.40	6.25	-1.89
141	5.99	30.12	6.86	6.10	-1.80
161	5.88	29.83	6.42	6.01	-2.24
181	5.78	29.59	6.05	5.95	-2.85
201	5.70	29.38	5.74	5.91	-3.55

Table 2. Theoretical versus measured internal inductance for stripline MCM geometry.

The lower resistance and small penetration depth of HTSC interconnects will result in:

$$L(f) = L_{ext}$$

$$R(f) = 2\pi f \times \mu_0 \times (\sigma_1 / \sigma_2) \times (\lambda / W)$$

where $\sigma_1 - j\sigma_2$ is the complex conductivity of the superconductor, λ is the penetration depth and W is the cross sectional width. So for $\sigma_1 << \sigma_2$ and $\lambda << W$, $R(f)$ can be small. Therefore, the result will be HTSC lines having both a faster propagation constant (due to L(f)) and lower loss (due to R(f)) than their normal metal counterparts.

Normal Metal Covering Layers

Previously in the section on magnetic flux penetration, mention has been made of the effect of losses due to covering layers of normal metal. This metal could be used for passivation, structural integrity, or to provide a redundant current path at HTSC grain boundaries. A quasi-static analysis of the surface impedance of a normal layer of metal atop a superconducting strip has been performed. The resulting expression depends on the thickness of the normal layer and the complex conductivity of both the normal and superconducting layers. The expression is;

$$R_{seff} = R_{sn} * F(T/\delta)$$

where

R_{seff} is the effective surface resistance
R_{sn} is the normal metal surface resistance
T is the thickness of the normal layer
δ is he skin depth of the normal layer

$$F(x) = \frac{\sinh 2(x-\alpha_R) + \sinh 2\alpha_R + \sin 2(x-\alpha_i) + \sin 2\alpha_i}{\cosh 2(x-\alpha_R) - \cos 2(x-\alpha_i)}$$

$$\alpha_R + j\alpha_i = \ln\left(\frac{\sqrt{\sigma} - \sqrt{\sigma_s}}{\sqrt{\sigma} + \sqrt{\sigma_s}}\right)$$

σ = Normal metal conductivity
σ_s = Superconductor complex conductivity

Note that as $T/\delta \to \infty$, $F(T/\delta) \to 1$, and the normal metal skin resistance is the effective resistance for thick layers (as one would expect).

Also, note that for $|\sigma_s| >> |\sigma|$

$$\alpha_R \approx 0 \quad \alpha_i \approx \pi/2$$

and

$$F(T/\delta) = \frac{\sinh(2T/\delta) - \sin(2T/\delta)}{\cosh(2T/\delta) + \cos(2T/\delta)}$$

which is zero to first order in T/δ. Therefore, <u>thin</u> covering films of normal metal should result in negligible surface loss.

Section 2.
Commercialization of High Temperature Superconducting Technology

The activities for this quarter centered around the completion of the first superconductive MCM teams and the initiation of the next two MCM teams. Additional efforts were spent to study the potential market for superconducting MCM, and per Dr. Patten, some efforts went into discussions with Epri on some market study for the bulk superconductivity.

Accomplishments

The first team led by E-System's Melpar Division has been completed with the addition of Data Max Corporation. This company consists of engineers who designed the ETA-10, a high performance computer that operated at 77 K. This knowledge and experience in building a low temperature computer system will prove extremely valuable for the SC-MCM technology development. Most likely Data Max will also participate with other MCM teams as they are formulated.

Currently, there are many companies involved in the DARPA superconductivity programs. Nearly all of these are universities or major companies and very few are dedicated merchant suppliers. Our attempt in forming the next two teams is to find additional merchant suppliers. In that regard, we did visit Emcore and spoke to ATM. Our visit to Emcore proved to be promising. Peter Norris and Norm Shoemaker seemed to be enthused about the MCM technology, as was the case with other merchant superconductor suppliers. Emcore has little experience in MCM technology. Recognizing the reality that we all face, namely R & D funds are limited, the question certainly keeps coming up regarding the survivability of these merchant suppliers. As a result, our thinking seems to be leaning toward the idea that maybe the merchant suppliers such as STI, Conductus, and Emcore should be included in all teams. They should receive technology benefits from all researchers and begin supplying products as soon as they are available. It is critical that this point not be overlooked.

We have tentatively looked at the various research contractors that might serve on the next two teams. Initial efforts are now used on targeting new team leaders that would play similar roles as E-Systems.

In addition to the MCM teams, an initial list has been tentatively organized for [illegible]e passive u-wave devices. All of these will be discussed wit[illegible]r. Patten and Dr. Wolf in early April.

Activities

Activities included many meetings with E-Systems, and several meetings with Data Max, STI, Conductus, MIT, Quad Design, Emcore, Boos-Allen and Cornell. Special sessions were held at n-Chip to look into the status of CAD tools for conventional MCM's and how they might be modified and applied to SC-MCM. Also, per Frank Patten's request, a bulk superconductivity conference was attended to evaluate the potentials of that market segment.

3.3 Q2 1991 Quarterly Report

Section 1.0

1.1. Background

A key question in the application of high temperature superconducting (HTSC) interconnects to advanced, very high density multi-chip modules (MCM's) is which HTSC material to use. Probably the best developed HTSC material is YBCO ("1-2-3"), but its transition temperature (T_c ~ 93°K) is about 30°K lower than that of "Thallium". Optimum performance of HTSC materials (eg., highest J_c, lowest R_s, etc.) are generally obtained at temperature below about 60% to 80% of T_c, though at the liquid nitrogen saturation temperature (T_{sat} = 77°K at 1 atmosphere), YBCO has shown more than adequate performance for MCM applications. However, if the HTSC operating temperature were substantially above 77°K, YBCO would not be useable.

In a visit to John Rowell and Randy Simon at Conductus on March 11, they relayed a concern expressed by Ted VanDuzer that YBCO might not be suitable for MCM interconnects due to the heat generated by the integrated circuit chips. More specifically, even when chips are immersed in 77°K liquid nitrogen, if their operating power density is reasonably high (as it is expected to be) the die temperatures may be substantially higher (eg. ~ 10°K or so) than the liquid nitrogen temperature. If the HTSC interconnects operate at the die temperature, then the HTSC operating temperature would be too close to the critical temperature of YBCO for that material to be useable in such MCM applications. If this were in fact true, this would be sad, since the state of development of the YBCO materials technology is quite advanced and it would be unfortunate to have to dismiss consideration of its use due to thermal limitations.

1.2. Thermal Analysis Approach

It was felt that the importance of the issue of HTSC material selection to the HTSC MCM effort is so great as to make it imperative to examine, on a quantitative basis, this thermal issue. The first step in the thermal analysis (carried out under separate support) was to do a preliminary 2-dimensional analysis to roughly simulate a cross-sectional view of the MCM. Roughly, in this case, means a linear, constant temperature (or insulating boundary condition 2-D analysis using a square-grid Gauss-Siedel relaxation method 2-D solver for Poisson's equation (as applied to heat flow). Because the actual problem is a constant power density (on the active surface of the IC chips), not a constant temperature, case, and the heat flow in the nucleate boiling process at the liquid nitrogen interfaces is a highly nonlinear process, not a linear one, the results could not be expected to be quantitatively precise. The results from this analysis indicated however, that for an ordinary two dimensional MCM with chips on one side of the MCM substrate only, the 3-dimensional nature of the physical MCM has very little influence on the worst-case HTSC interconnect temperature. In other words, even though the sides of the IC die and the HTSC interconnect layers in the gaps between the die subject to liquid nitrogen) cooling in addition to the face of the die and the bottom side of the MCM substrate, the HTSC temperature under the center of the die is not much lower than what would be obtained from a one-dimensional analysis assuming an indefinitely large die size. Hence the analysis undertaken here, for which the thermal model shown in Fig.1 was derived, is a worst-case one-dimensional, nonlinear analysis.

1.3 Liquid Nitrogen Heat Transfer Characteristics in an MCM Context

Extensive evaluation of the heat transfer characteristic of cryogenic fluids such as liquid nitrogen has been carried out. Marty Nisenhof of NRL was kind enough to provide a copy of the K ane, et.al. article (R.J. Krane , J.R. Parsons and A. Bar-Cohen, "Design of a Candidate Thermal Control System for a Cryogenically Cooled Computer", IEEE Transactions on Components, Hybrids, and Mfg. Tech, Vol. 11, No 4, Dec. 1988, pp 545-556) from which the liquid nitrogen pool boiling data used here was derived. Fig. 2 shows a log-log plot of the power density or heat flux (in W/cm^2) measured from the surface of a 1" copper sphere immersed in liquid nitrogen (abbreviated LN_2 here), versus the temperature of the copper surface relative to the liquid nitrogen temperature, $\Delta T = T - T_{sat}$, where T_{sat} is nominally 77°K. There are two principal operating regions shown on this curve: the high heat flux, low ΔT region on the left, called the nucleate boiling region (ΔT below 10°K to 20°K), and the (very undesirable) high ΔT, low P/A region above ΔT = 30°K (film boiling region), connected by a negative resistance "transition boiling region (~20°K to 30°K). It should be noted that details of this curve are probably dependent on geometry, surface material and finish, etc. of the heater, but the general features should apply. It should also be noted that these are steady-state curves, measured when nucleate boiling is fully developed. As noted in the Krane article (and first pointed out to by Lou Colonna-Romano of DEC in a helpful discussion), when the heater power is first applied, the heat transfer mechanism takes a finite amount of time or "over temperature" to go into fully developed nucleate boiling. During this interval the heat transfer will essentially be convective, which, in a free-convection (as opposed to a forced convection, pumped fluid) case has relatively poor thermal resistance. For example, for a vertical wall at temperature, T_w, in still LN_2 at a temperature, T_{liquid}, Krane estimates the convective heat transfer as

$$P/A = 0.0161 (T_w - T_{liquid})^{1.333} \qquad \text{Eq. 1}$$

where P/A is in W/cm^2, and the temperatures are, as usual, in °K. Note, for example, that for no liquid subcooling ($T_{liquid} = T_{sat} = 77$°K nominal), at $\Delta T = 10$°K the convective heat transfer (prior to nucleate boiling) would only be P/A = 0.35 W/cm^2, in comparison to P/A = 11 W/cm^2 in fully developed nucleate boiling (Fig. 2). By subcooling the LN_2 (subcooling to 63°K is possible before freezing begins), the convective contribution would be greatly increased at any given temperature. This could also be achieved with using forced convection, by pumping the liquid at a substantial velocity. (One theory is that nucleate boiling gives its very high heat transfer due to the very high liquid agitation and corresponding local liquid velocities in the surface region, which means that similar fluxes should be attainable with forced convection if the boundary layer is thin enough).

The reason for bringing this issue of forced convection, or other than simple pool boiling up in this HTSC MCM context is that the bare-chip power densities that would be involved in MCM cooling are much higher than those involved in the ETA 10 cryogenically cooled supercomputer. While the packaged devices (~ 1" square) in the ETA 10 operated at something of the order of 0.25 to perhaps 0.5 W/cm^2, higher speed bare die in an MCM might be running at up to 5 to 10 W/cm^2 in CMOS, or higher in higher performance technologies. While in the ETA 10, operation was in the "unconditionally stable" region of Fig. 2 where ΔT is a single-valued function of P/A, at higher power densities we will be in the multi-valued region. Here it is conceivable that upon power-up, thermal overshoot could give a transition directly into the catastrophic film boiling region under unfavorable conditions. It seems likely that straightforward measures such as submersed jet forced convection, used in combination with nucleate boiling, can easily cope with such potential problems, but the issue should be examined, particularly if fairly high power density (eg. > 5 W/cm^2) chips are to be considered for use.

1.4. HTSC MCM One Dimensional Analysis/Thermal Model

The HTSC MCM configuration analyzed was shown with the worst-case one dimensional thermal model in Fig. 1. The structure is assumed fabricated on a 1mm thick substrate of either CaF_2 (K = 38.9 W/m°K at 77°K) or Mg0 (77° thermal conductivity, k, estimated at 200 W/m°K). (I don't have the k for $LaA10_3$, and for our purposes, either sapphire or silicon have essentially infinite 77°K thermal conductivities, if they were to be used). The HTSC layers (relatively thin, so with presumably negligible thermal resistance) are on top of the substrate and the IC chip is mounted directly to it using a thickness of epoxy die attach material. The active (power-generating) surface of the 25-mil thick IC chip to be at the top, but this is essentially irrelevant since the thermal conductivity of silicon at 77°K (1400 W/m°K) is so high. In terms of the electrical-analogue model at the right of Fig. 1, the chip power, P/A, is represented as a current source into the upper (T_{chip}) node.

The critical factor in the physical MCM structure is the thickness and thermal conductivity of the organic die attach layer. In most norm. al IC's, silver-loaded (or sometimes diamond-loaded) epoxy die attach materials are used for enhanced thermal conductivity over unloaded materials. For example, at room temperature, silver-epoxy has k = 5.8 W/m°K (or 8.7 W/m°K for diamond-loaded epoxy), while unloaded epoxy has k = 0.4 W/m°K typical, and polyamide has k = 0.2 W/m°K. The epoxy thicknesses typically used are of the order of 3 mils (0.0762 mm) for modest sized VLSI die, or 6 mils (0.1524 mm) for larger die sizes (the greater thicknesses accommodating greater thermal expansion mismatch strains with minimal stress). For our HTSC MCM case, we do not plan to take heat out through the substrate, but rather directly from the die to the LN_2, so we have no reason to reduce the thermal resistance,

$$R_{th} = \Delta T/(P/A) = z/k \qquad \text{Eq.2}$$

(where z is the thickness and k the thermal conductivity) of the die attach layer. On the contrary, we prefer to have this layer be as insulating as possible, since (referring to the electrical equivalent of the thermal model at the right of Fig. 1) the temperature at the HTSC layer, T_{HTSC}, will be reduced as R_{Epoxy} is increased. Hence we want to

use unloaded epoxy (perhaps enhanced with thick polyamide coatings on the HTSC and/or die backside surfaces) die attach material in as thick a layer as practical. For the purposes of the analysis, a 77°K thermal conductivity of 0.4 W/m°K was assumed with die attach layer thicknesses of 1 mil, 3 mils, 6 mils, 12 mils and 24 mils analyzed. (Obviously, from Eq. 2, 6 mils of k = 0.2 polyamide would be equivalent to 12 mils of k = 0.4 epoxy, etc.).

As indicated by Eq. 2, the solid materials comprising the MCM are assumed to have linear heat flow characteristics, such as illustrated in Eq. 2. In the preliminary 2-D heat flow analysis described earlier, a fixed R_{th} was also assigned to the solid wall to liquid nitrogen conductances at the top and bottom of Fig. 1. For example, if we assume P/A = 10 W/cm^2 and refer to Fig. 2 we find $\Delta T = T - T_{sat} = 9.68°K$ or an effective $R_{th} = 0.968°K/W/cm^2$). If we take as an example a 1mm MgO substrate ($R_{sub} = 0.05$), with a 6 mil epoxy die attach thickness ($R_{Epoxy} = 3.81$ from Eq. 2) and $R_{sub} = 0.00454$ for the 25 mil thick silicon die, using the effective $R_{th} = 0.968$ values for the upper and lower LN_2 interfaces (shown as diodes in Fig. 1), we get an IC die surface temperature rise of $\Delta T_{chip} = 8.065°K$ (above $T_{sat} = 77°K$) and an HTSC layer temperature rise of only $\Delta T_{HTSC} = 1.7°K$. In fact, however, as the nonlinear analysis will show, the actual HTSC temperature rise for this case is more than twice this high ($\Delta T_{HTSC} = 3.9°K$, as will be shown in Fig. 11) This is because the heat flow at the LN_2 interface is highly nonlinear. Under the conditions of this example the effective R_{th} at the interface at the bottom of the substrate is not 0.968°K/(W/cm^2), but rather is closer to 2.8°K/(W/cm^2) due to the lower thermal flux at this surface (the results of the relatively high thermal resistance of the epoxy). Hence, a nonlinear analysis is necessary to obtain reasonable accuracies for ΔT_{HTSC}.

In the calculations, a statistical fit was made to the left (nucleate boiling) portion of the liquid nitrogen pool boiling curve of Fig. 2. For $1°K \leq \Delta T \leq 10°K$, a good fit was found to be

$$(P/A) = 0.0749\ \Delta T^{2.156} \qquad \text{Eq. 3}$$

where as usual, P/A is in W/cm$_2$ and $\Delta T = T - T_{sat}$ is in °K. For the computer analysis, if the nucleate boiling P/A exceeds that due to convection (Eq. 1), then Eq. 3 is used for the nonlinear LN_2 interface conductances in the model of Fig. 1. Since for the cases treated, no liquid subcooling was assumed ($T_{liquid} - T_{sat}$ = 77°K nominal), this was always the case in the range of P/A's treated.

1.5. Results of 1-D Thermal Model Calculations for HTSC MCM

A computer program was written to solve the nonlinear heat flow model shown in Fig. 1. In the electrical analog model show at the right in Fig. 1, the chip power is represented by a current incident in the top node (T_{chip}), and the voltages at each node represent the temperature rise above saturation at that point. The program was, for convenience, written in QuickBasic for the MacIntosh IIFX, with output in EXCEL for format as a simple way to obtain graphics output. Figs. 3-8 apply to the 1mm thick CaF_2 substrate case, and Figs. 9-12 apply for a 1mm thick MgO substrate (and are reasonably accurately representative of any higher thermal conductivity substrate material such as sapphire or silicon). As was mentioned previously, the critical factor in the calculations is the thickness and thermal conductivity of the epoxy die attach layer. Fig. 3, for example, shows the case for a 3-mil layer, assuming k_{Epoxy} = 0.4 W/m°K. The left hand column represents the total chip power dissipation, the extreme right column the portion of that power going directly into the nitrogen at the top (Silicon - LN_2) interface, and the third column from the left, T_{chip}, is the temperature of that interface. The second column from the right shows the portion of the chip power going down through the epoxy, HTSC layers and the substrate into the LN_2 at the bottom surface, and the third column from the right shows the temperature, $T_{substrate}$, of that bottom interface. The goal of the whole calculation, of course, is to determine the temperature of the HTSC interconnects, which is just $T_{substrate}$ plus the fairly small temperature drop across the substrate, $\Delta T_{sub} = (P/A)_{sub} + R_{sub}$. For convenience, the thermal resistances of the substrate, epoxy and silicon chip regions ar shown just above the column printouts, along with their sum, R_{total}. We note from Fig. 1, for example, that at a 10 W/cm^2 chip power, 80.5% of the power goes directly into the LN_2 at the upper surface, and 19.5% goes down through the substrate. Because of

the nonlinear nature (Eq. 3 or Fig. 2) of the nucleate boiling thermal transfer, the difference between the upper and lower LN_2 interface temperatures (upper and lower curves in Fig. 4) is less than a factor of 2 in spite of the fact that power densities are over a factor of 4 different. This is unfortunate, since it raises the HTSC temperature (solid line in Fig. 4) higher than one might hope based on the thermal resistances.

By further increasing the thickness of the epoxy layer to, for example, 24 mils (more practically achieved with a 12 mil thick polyamide [k = 0.2 W/m°K] layer, or perhaps by using a thinner epoxy preform with holes in it), the power split at P/A = 10 W/cm^2, as shown in Fig. 5, can be shifted further, with 95.4% going out the top surface and only 4.6% going out through the substrate side. As shown in Fig. 6. this has the desired effect of significantly reducing the temperature of the substrate and HTSC layers, to about 25% of the die temperature, but this is still higher than one could hope. Note that the temperature drop across the substrate itself is only 0.1185°K for this case (or 0.5° for the 3 mil epoxy case of Fig. 3), so changing to a much higher thermal conductivity substrate will not change the HTSC temperature by very much as long as the substrate cooling is simple pool boiling (as opposed to forced convection).

Fig. 7 summarizes the chip and HTSC temperature for the 1mm CaF_2 substrate example with epoxy thicknesses of 1, 3, 6, 12 and 24 mils. This data is graphed in Fig. 8.0. Obviously, from Fig. 1, if the epoxy is made thin enough, T_{HTSC} will nearly equal T_{chip}. This is demonstrated in the curves shown in Fig. 8.

This set of calculations was also carried out for higher thermal conductivity, MgO substrate case (k estimated at 200 W/m°K at 77°K), with results shown in Figs. 9-12. Fig. 10 shows, for example, that even for the 3 mil epoxy case, the temperature drop across the substrate at P/A = 10 W/cm^2 is only 0.1°K, but that the temperature of interest at the HTSC layer is only 0.276°K lower than for the CaF_2 substrate case (Figs. 3 and 4). Fig. 11 summarizes the MgO substrate results for the same set of epoxy thicknesses as shown for CaF_2 in Fig. 7, and the temperature rises are plotted in Fig. 12. While the HTSC temperatures for MgO in Fig. 12 are somewhat lower than for CaF_2, the differences are rather small, except for cases with very thin epoxy layers.

1.6. Conclusions

If we take, as atypical configuration, an MgO substrate and 6 mil epoxy (without silver or diamond filling, of course) die attach case, with simple pool boiling (the MCM sitting vertically in a pool of liquid nitrogen), the worst case (die center) temperature rise of the HTSC layer above the T_{sat} = 77°K liquid nitrogen saturation temperature will vary (Fig. 12) from about 2.33°K at a P/A = 2 W/cm^2 chip power density to 3.15°K at 5 W/cm^2, or up to 4°K at 11 W/cm^2 if one dared to operate so close to the maximum power density for nucleate boiling (about 13.9 W/cm^2). A 4°K temperature rise should be expected to quite significantly degrade the performance of YBCO HTSC interconnects, though possibly not catastrophically.

However, it is probably not necessary to accept 81°K operation of the HTSC layers rather than 77°K. By employing forced convections cooling of the MCM, at least on the substrate side, it may well be possible to reduce greatly the substrate (and hence HTSC layer) temperature rise. In fact, with careful epoxy die attach layer design (ie, incorporation of polyamide or "holes" in somewhat thicket die attach structures, it might be possible to reduce the substrate-side power load to only 5% to 10% of the chip power. Hence the liquid nitrogen supply to the substrate side could be subcooled with not very much additional cooling energy cost, and operation of the HTSC layers at well under 77°K obtained. Some of these possibilities need further consideration, but the prognosis for the use of YBCO for HTSC MCMs looks generally good at this point.

One-Dimensional Thermal Model for HTSC MCM
Liquid Nitrogen Pool Boiling Cooled

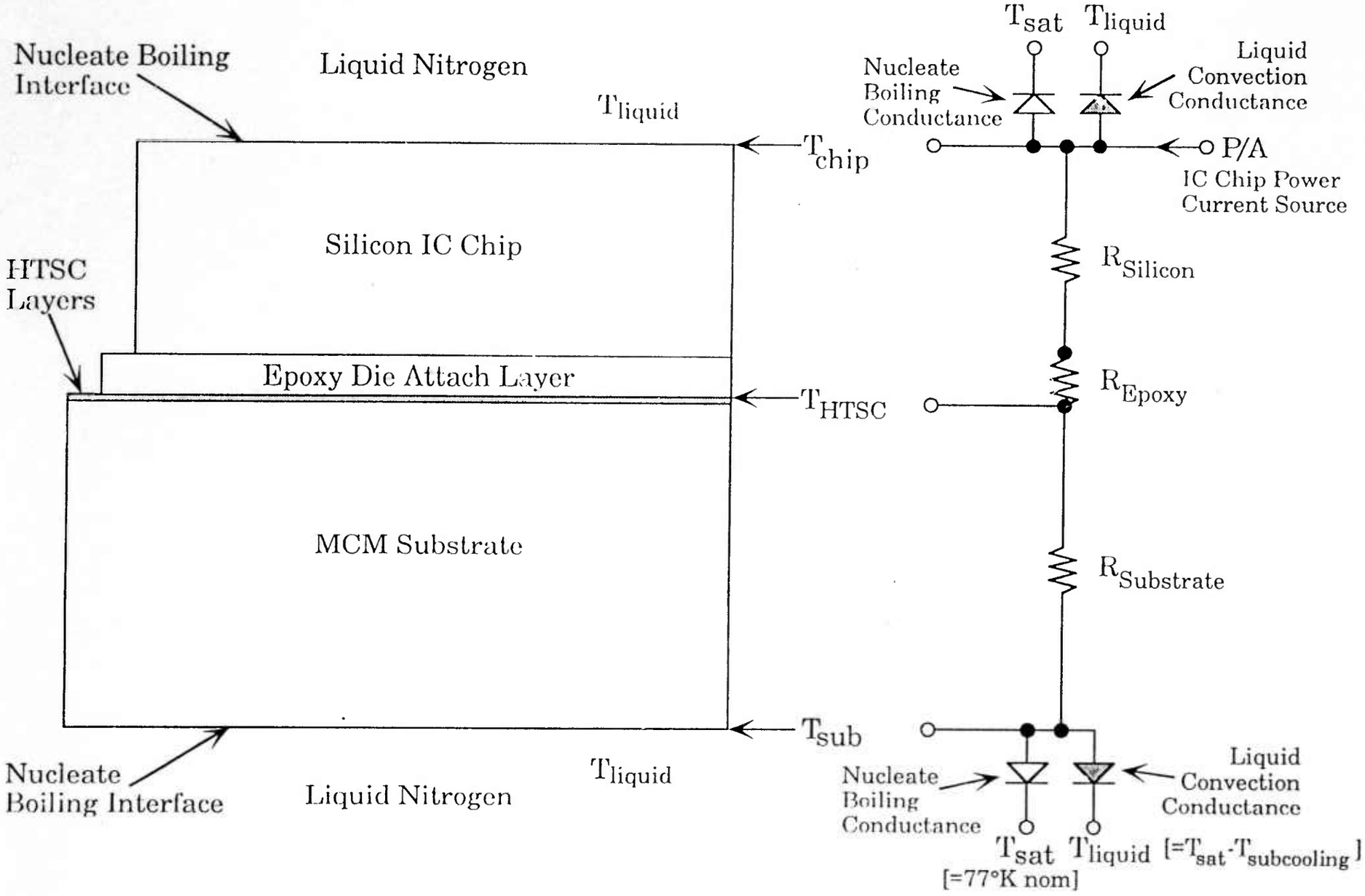


Figure 1

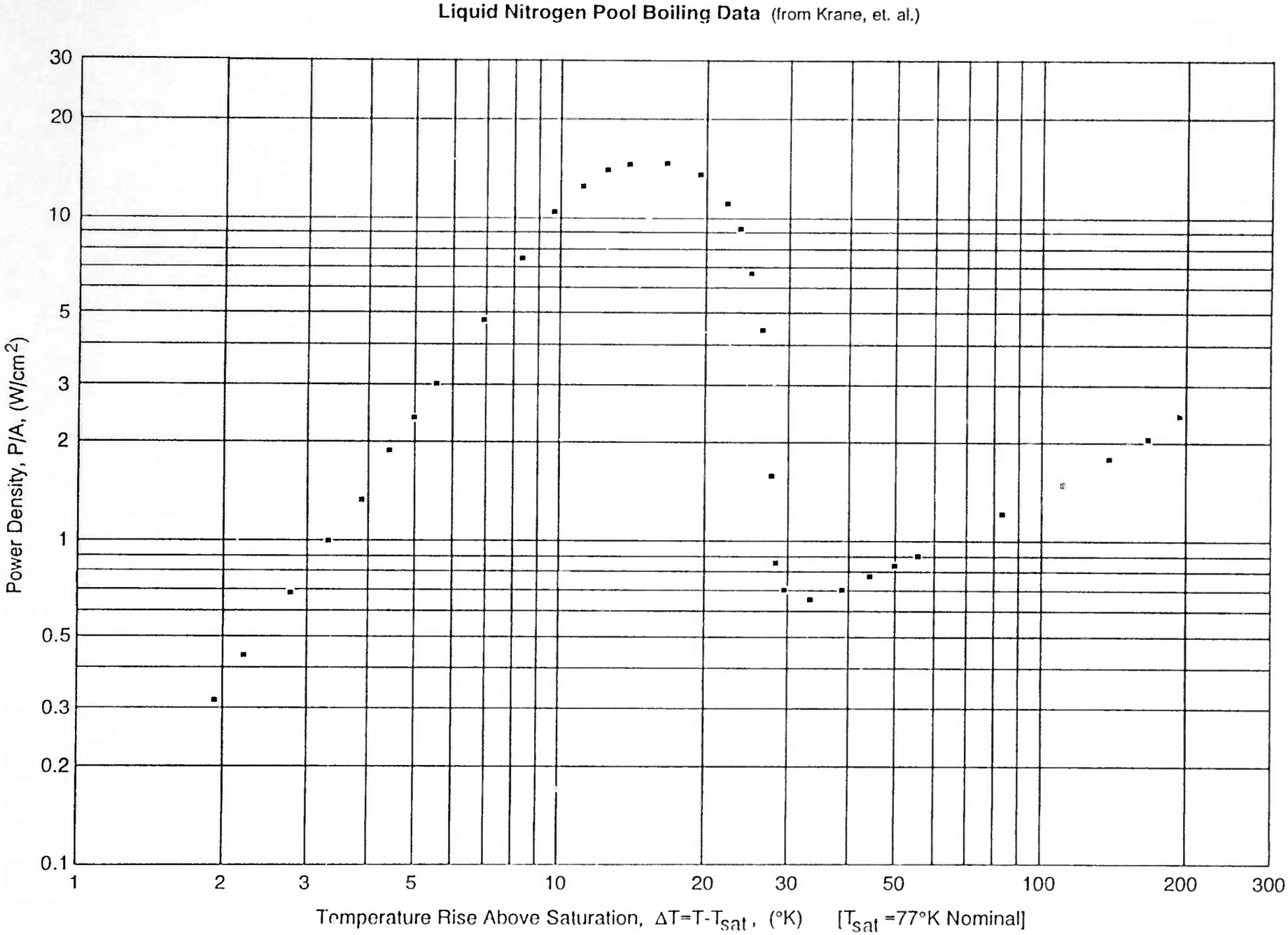

Liquid Nitrogen Pool Boiling Data (from Krane, et. al.)
Power Density, P/A, (W/cm2)
30
20
10
5
3
2
1
0.5
0.3
0.2
0.1
1
2
3
5
10
20
30
50
100
200
300
Temperature Rise Above Saturation, ΔT=T-Tsat, (°K) [Tsat =77°K Nominal]

Figure 2

Calculation of HTSC Temperature vs. P/A in MCM with LN2 Nucleate Boiling R. C. Eden June 1991
1-D Calculation of HTSC ΔT in Nucleate Boiling LN2 Cooled MCM [ΔT=T-Tsat where Tsat=77°K nom].
Convective-Nucleate Xover @ ΔTX= .154292482 °K @ P/A= 0.0013323517 W/cm^2, without N2 subcooling.

Thermal Conductivity of Epoxy Die Attach (e.g. 0.4W/m °K), KEPX= .40000
Thickness of Epoxy Die Attach in mils, Zepoxy= 3 (or 7.620016E-02 mm)
Si Chip Thickness, Zchip= .635 mm, Zsubstrate= 1 mm, Zepoxy= .003 inches

MCM Substrate Material is CaF2 with Thermal Conductivity of Ksub= 38.9000 W/m°K
For 1 cm^2 area, the Thermal Resistances (in °K/W-cm^2) are:
RSI= 4.535714E-03 REPXY= 1.905004 RSUB= .2570694 RTOT= 2.166609

P/A[W/cm^2]=	T(HTSC)°K=	T(chip)°K=	T(Substrt)=	P/A(Substrt)	P/A(Chip-N2)
0.1	0.7912229	0.8749327	0.7799536	0.0438377	0.05616229
0.15	0.9450225	1.066956	0.9286073	0.0638548	0.08614521
0.2	1.070615	1.229286	1.049255	0.08309344	0.1169066
0.25	1.178482	1.372679	1.152338	0.1016983	0.1483016
0.3	1.273928	1.502625	1.24314	0.1197657	0.1802343
0.4	1.438933	1.734051	1.399203	0.1545491	0.2454509
0.5	1.579964	1.938635	1.531678	0.1878315	0.3121685
0.6	1.704258	2.1241	1.647737	0.2198659	0.3801342
0.7	1.816061	2.295034	1.75158	0.2508318	0.4491682
0.8	1.918109	2.45443	1.845908	0.2808641	0.519136
0.9	2.012282	2.604369	1.932573	0.3100678	0.5899321
1	2.099938	2.746369	2.012913	0.3385275	0.6614724
1.5	2.469115	3.369936	2.347843	0.4717478	1.028252
2	2.763966	3.897056	2.611425	0.5933837	1.406616
2.5	3.013048	4.362027	2.831444	0.7064419	1.793558
3	3.230595	4.782575	3.021662	0.8127508	2.187249
4	3.601122	5.529144	3.341565	1.009679	2.990321
5	3.912951	6.186266	3.606909	1.190504	3.809496
6	4.184581	6.779549	3.835237	1.358949	4.64105
7	4.426673	7.324297	4.036583	1.517447	5.482553
8	4.645996	7.830534	4.217282	1.667699	6.332301
9	4.847146	8.305243	4.381604	1.810958	7.189042
10	5.033401	8.753528	4.532584	1.948179	8.051821
11	5.207189	9.179247	4.672456	2.080113	8.919888

Figure 3

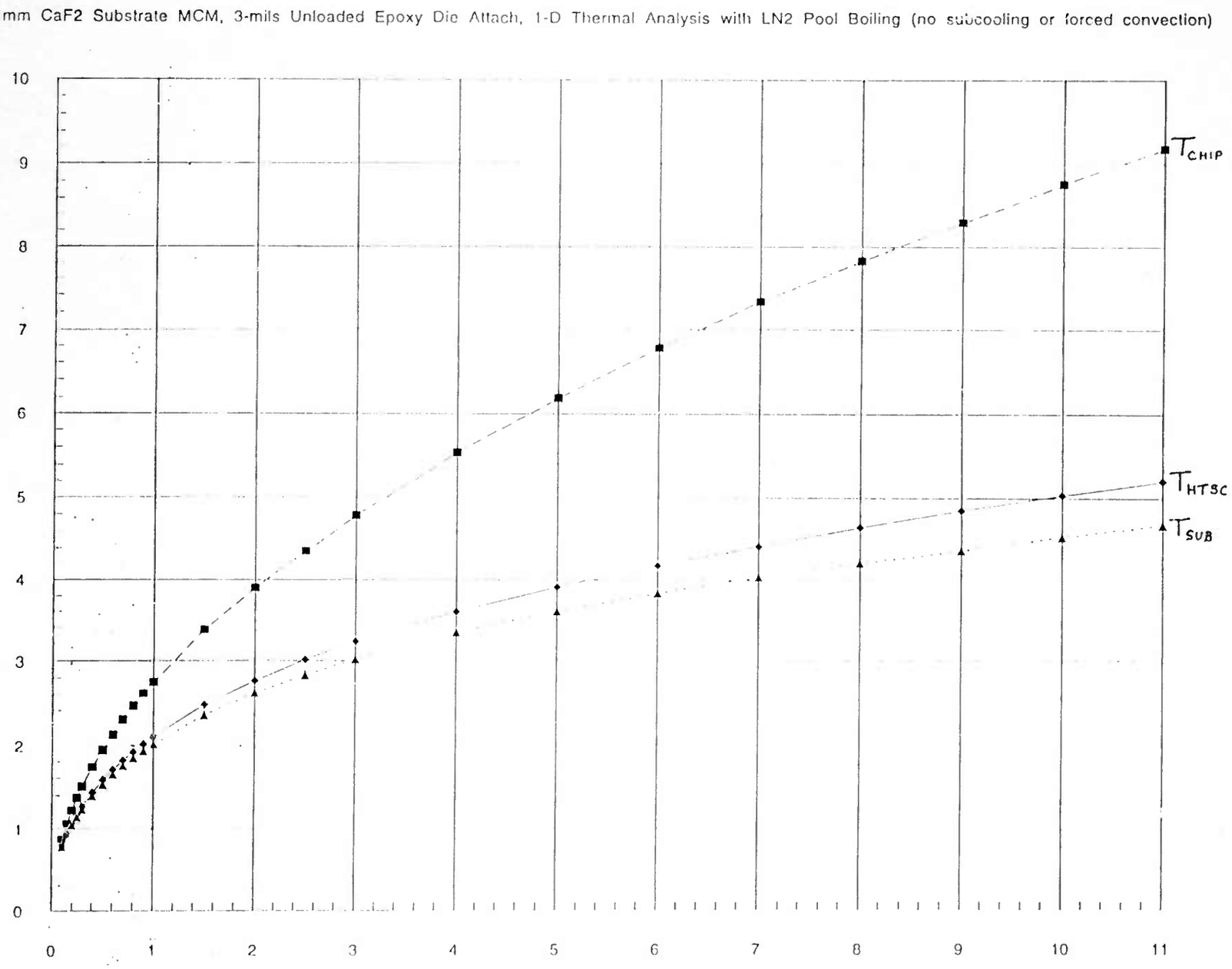

1mm CaF2 Substrate MCM, 3-mils Unloaded Epoxy Die Attach, 1-D Thermal Analysis with LN2 Pool Boiling (no subcooling or forced convection)
10
9
8
7
6
5
4
3
2
1
0
0
1
2
3
4
5
6
7
8
9
10
11
T_{CHIP}
T_{HTSC}
T_{SUB}
Horizontal is Chip Power Density in W/cm^2, Vertical is ΔT=T-Tsat [Tsat=77°K nom] for IC chip, HTSC layers and Substrate (T-B)

Figure 4

Calculation of HTSC Temperature vs. P/A in MCM with LN2 Nucleate Boiling R. C. Eden June 1991
1-D Calculation of HTSC ΔT in Nucleate Boiling LN2 Cooled MCM [ΔT=T-Tsat where Tsat=77°K nom].
Convective-Nucleate Xover @ ΔTX= .1542924 °K @ P/A= 0.0013323517 W/cm^2, without N2 subcooli

Thermal Conductivity of Epoxy Die Attach (e.g. 0.4W/m °K), KEPX= .4000 W/m°K
Thickness of Epoxy Die Attach in mils, Zepoxy= 24 (or .6096013 mm)
Si Chip Thickness, Zchip= .635 mm, Zsubstrate= 1 mm, Zepoxy= .024 inches

MCM Substrate Material is CaF2 with Thermal Conductivity of Ksub= 38.900 W/m°K
For 1 cm^2 area, the Thermal Resistances (in °K/W-cm^2) are:
RSI= 4.535714E-03 REPXY= 15.24003 RSUB= .2570694 RTOT= 15.50164

P/A[W/cm^2]=	T(HTSC)°K=	T(chip)°K=	T(Substrt)=	P/A(Substrt)	P/A(Chip-N2)
0.1	0.6116453	0.9982979	0.6051252	0.0253633	0.0746367
0.15	0.7034557	1.224105	0.694676	0.03415309	0.1158469
0.2	0.7747685	1.413915	0.7639906	0.04192617	0.1580738
0.25	0.8337963	1.580619	0.8212026	0.04898943	0.2010106
0.3	0.8845318	1.730874	0.8702599	0.0555176	0.2444824
0.4	0.9693643	1.996543	0.9520429	0.06738	0.33262
0.5	1.03937	2.229415	1.019302	0.07806357	0.4219364
0.6	1.099418	2.439004	1.076829	0.08787302	0.512127
0.7	1.152263	2.630972	1.127328	0.09699906	0.603001
0.8	1.199626	2.809009	1.172487	0.1055709	0.6944291
0.9	1.24266	2.975678	1.213436	0.113681	0.786319
1	1.282179	3.132846	1.250972	0.1213984	0.8786016
1.5	1.443708	3.816107	1.403702	0.1556226	1.344377
2	1.567967	4.386279	1.520441	0.1848733	1.815127
2.5	1.670267	4.884655	1.616063	0.2108547	2.289145
3	1.757906	5.332317	1.697631	0.2344711	2.765529
4	1.904032	6.121005	1.832922	0.2766213	3.723379
5	2.024377	6.809978	1.943678	0.3139217	4.686079
6	2.127517	7.428597	2.038125	0.3477357	5.652265
7	2.218261	7.994207	2.120862	0.3788855	6.621115
8	2.299598	8.518053	2.194736	0.407913	7.592087
9	2.37352	9.007915	2.261644	0.4351973	8.564803
10	2.441432	9.469436	2.322919	0.4610168	9.538983
11	2.50436	9.906858	2.379532	0.4855826	10.51442

Figure 5

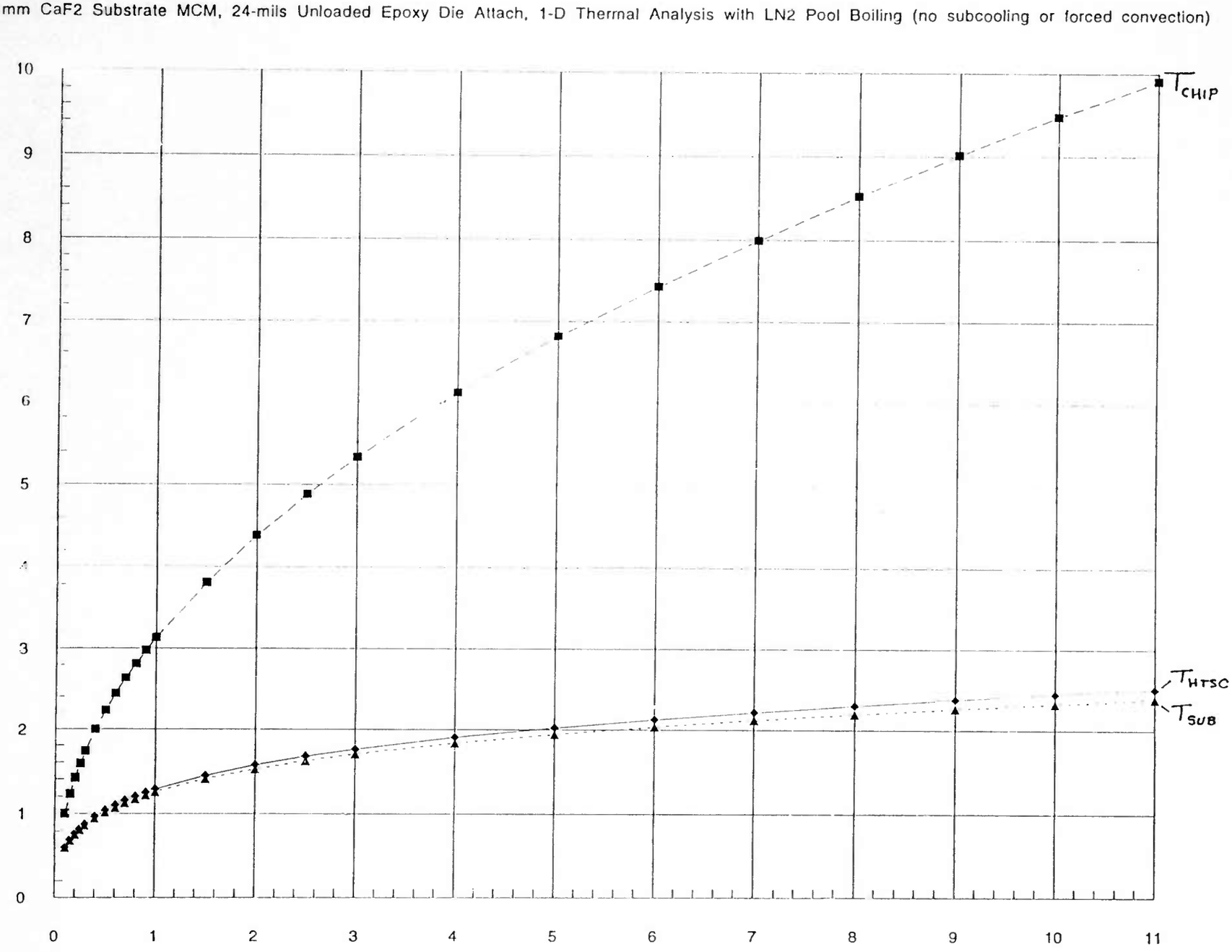

1mm CaF2 Substrate MCM, 24-mils Unloaded Epoxy Die Attach, 1-D Thermal Analysis with LN2 Pool Boiling (no subcooling or forced convection)
10
9
8
7
6
5
4
3
2
1
0
0
1
2
3
4
5
6
7
8
9
10
11
T CHIP
T HTSC
T SUB
Horizontal is Chip Power Density in W/cm^2, Vertical is ΔT=T-Tsat [Tsat=77°K nom] for IC Chip, HTSC layers and Substrate (T-B)

Figure 6

Summary of CaF2 Substrate MCMs with Various Epoxy Thicknesses

Calculation of HTSC Temporaturo vs. P/A in MCM with LN2 Nucloate Boiling R. C. Eden June 1991
1-D Calculation of HTSC ΔT in Nucleate Boiling LN2 Cooled MCM [ΔT=T-Tsat where Tsat=77°K nom].
Convective-Nucleate Xover @ ΔTX= .154292482034247 °K @ P/A= 1.332351724254022D-03 W/cm^2, without N2 subcooling.

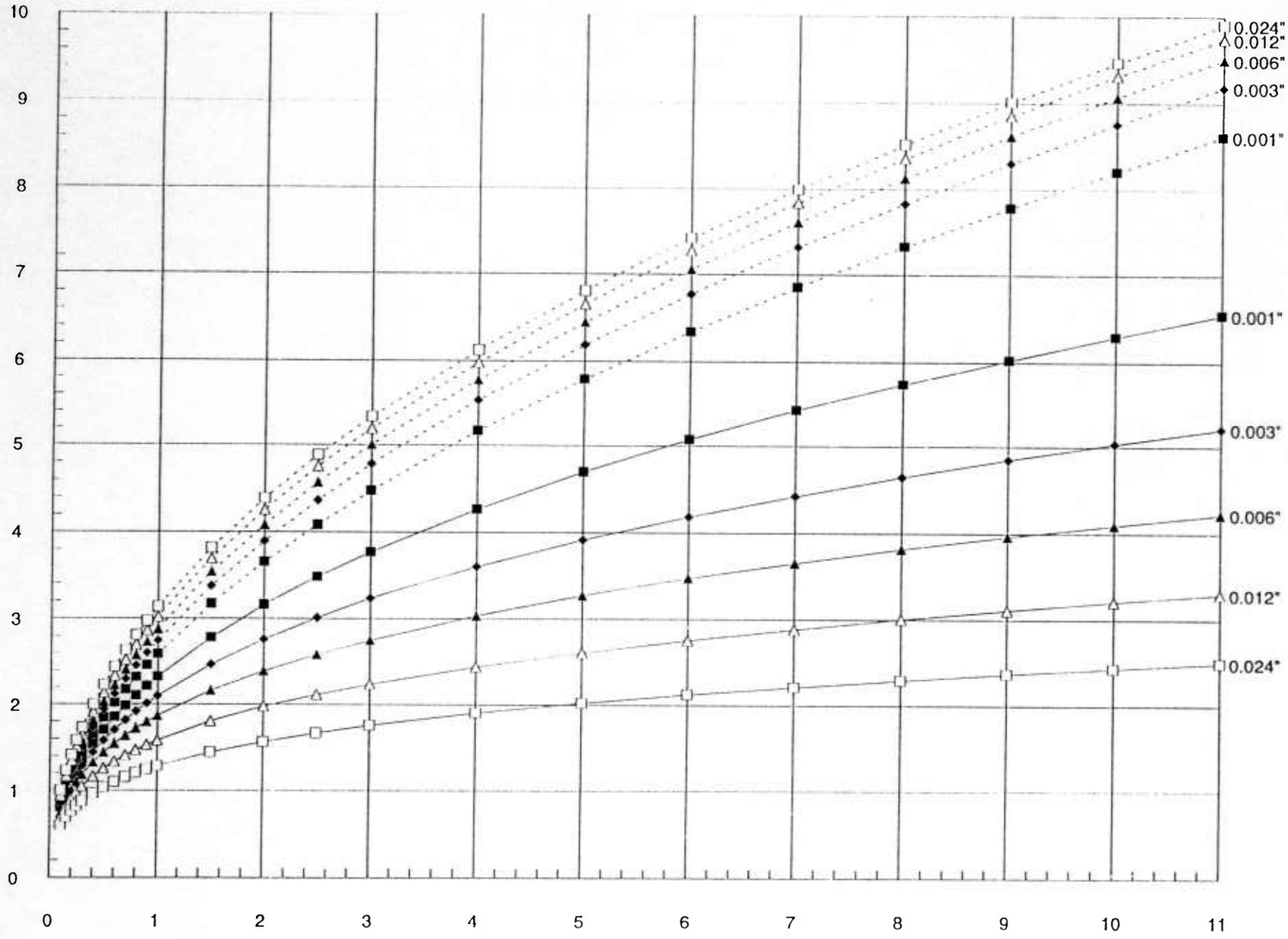
Thermal Conductivity of Epoxy Dio Attach (e.g. 0.4W/m °K), KEPX= .4000000059604645
Thickness of Epoxy Die Attach in mils, Zepoxy= 1 (or 2.540005E-02 mm)
Si Chip Thickness, Zchip= .635 mm, Zsubstrate= 1 mm, Zepoxy= .001 inches

MCM Substrate Material is CaF2 with Thermal Conductivity of Ksub= 38.90000152587891 W/m°K
For 1 cm^2 area, the Thermal Resistances (in °K/W-cm^2) are:
RSI= 4.535714E-03 REPXY= .6350013 RSUB= .2570694 RTOT= .8966064

	1mil Epoxy		3- mils Epoxy		6 mils Epoxy		12 mils Epoxy		24 mils Epoxy	
P/A[W/cm^2]=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=
0.1	0.8196688	0.8498849	0.7912229	0.8749337	0.7540688	0.9050652	0.6945382	0.9479737	0.6116453	0.9982979
0.15	0.9866067	1.031333	0.9450225	1.069956	0.8922779	1.107996	0.8110576	1.163319	0.7034557	1.224105
0.2	1.124874	1.183847	1.070615	1.22928	1.003411	1.279869	0.9030369	1.345292	0.7747685	1.413915
0.25	1.24503	1.318025	1.178482	1.372679	1.097702	1.431797	0.9800191	1.505761	0.8337963	1.580619
0.3	1.352435	1.439255	1.273928	1.502625	1.180299	1.56949	1.046734	1.650861	0.8845318	1.730874
0.4	1.540511	1.654472	1.438933	1.734051	1.321363	1.814602	1.159282	1.908364	0.9693643	1.996543
0.5	1.70366	1.84417	1.579964	1.938635	1.440325	2.031051	1.252986	2.134937	1.03937	2.229415
0.6	1.849267	2.015815	1.704258	2.1241	1.54404	2.227011	1.333881	2.339441	1.099418	2.439004
0.7	1.981685	2.173817	1.816061	2.295034	1.636494	2.407367	1.405428	2.527174	1.152263	2.630972
0.8	2.103732	2.321039	1.918109	2.45443	1.720229	2.575316	1.469808	2.701601	1.199626	2.809009
0.9	2.217353	2.459461	2.012282	2.604369	1.796984	2.733089	1.528498	2.86514	1.24266	2.975678
1	2.323957	2.590522	2.099938	2.746369	1.868002	2.882318	1.582545	3.019553	1.282179	3.132846
1.5	2.781716	3.166161	2.469115	3.369936	2.163049	3.535434	1.804767	3.692692	1.443708	3.816107
2	3.157168	3.653506	2.763966	3.897056	2.394575	4.084896	1.976933	4.256205	1.567967	4.386279
2.5	3.480855	4.084321	3.013048	4.362027	2.587732	4.567763	2.119338	4.749747	1.670267	4.884655
3	3.768248	4.474875	3.230595	4.782575	2.754831	5.003182	2.241751	5.193684	1.757906	5.332317
4	4.267321	5.170501	3.601122	5.529144	3.036415	5.773446	2.446617	5.976921	1.904032	6.121005
5	4.696197	5.785308	3.912951	6.186266	3.270811	6.448954	2.615973	6.66203	2.024377	6.809978
6	5.076006	6.342403	4.184581	6.779549	3.473308	7.057146	2.761529	7.27773	2.127517	7.428597
7	5.419148	6.855566	4.426673	7.324297	3.652602	7.614358	2.889882	7.841038	2.218261	7.994207
8	5.733614	7.3338	4.645996	7.830534	3.814155	8.131248	3.005146	8.363012	2.299598	8.518053
9	6.024905	7.783385	4.847146	8.305243	3.961641	8.615223	3.110076	8.851316	2.37352	9.007915
10	6.296989	8.208908	5.033401	8.753528	4.097665	9.071675	3.206613	9.311515	2.441432	9.469436
11	6.55284	8.613842	5.207189	9.179247	4.224142	9.504676	3.29618	9.747802	2.50436	9.906858

Figure 7

Summary of 1mm CaF2 Substrate MCMs with 1, 3, 6, 12 and 24 mils Epoxy Die Attach Thickness, LN2 Pool Boiling Only



Horizontal is Chip Power Density In W/cm^2, Vertical is ΔT=T-Tsat [Tsat=77°K nom] for IC Chip (Top) and HTSC Interconnect Layers (Bottom)

Figure 8

MgO Substrate

Calculation of HTSC Temperature vs. P/A in MCM with LN2 Nucleate Boiling R. C. Eden June 1991
1-D Calculation of HTSC ΔT in Nucleate Boiling LN2 Cooled MCM [ΔT=T-Tsat where Tsat=77°K nom].
Convective-Nucleate Xover @ ΔTX= .15429248 °K @ P/A= 0.00133235172 W/cm^2, w/o N2 subcooling

Thermal Conductivity of Epoxy Die Attach (e.g. 0.4W/m °K), KEPX= .40000 W/m°K
Thickness of Epoxy Die Attach in mils, Zepoxy= 3 (or 7.620016E-02 mm)
Si Chip Thickness, Zchip= .635 mm, Zsubstrate= 1 mm, Zepoxy= .003 inches

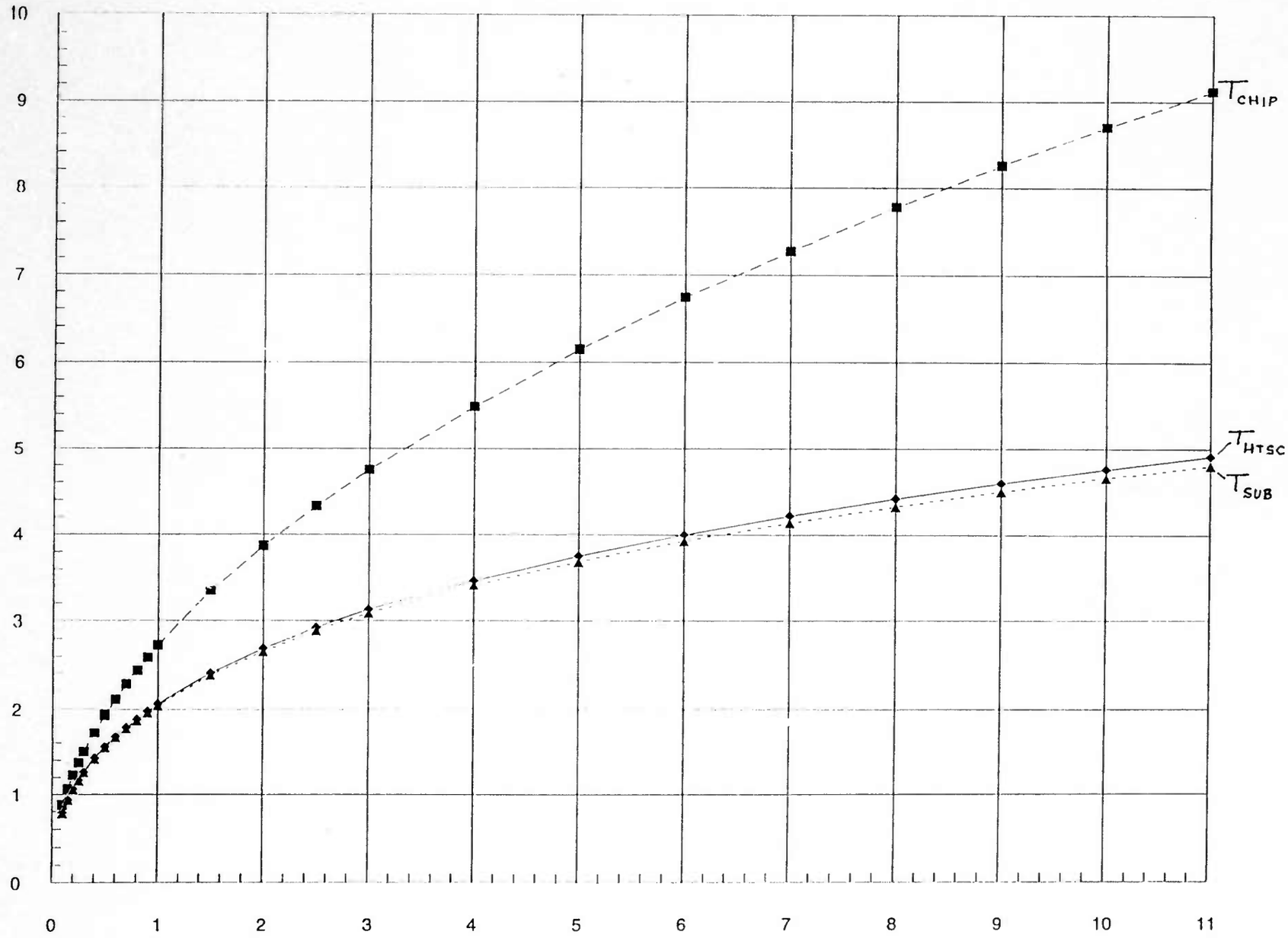
MCM Substrate Material is MgO with Thermal Conductivity of Ksub= 200 W/m°K
For 1 cm^2 area, the Thermal Resistances (in °K/W-cm^2) are:
RSI= 4.535714E-03 REPXY= 1.905004 RSUB= .05 RTOT= 1.95954

3 mils Unloaded Epoxy

P/A[W/cm^2]=	T(HTSC)°K=	T(chip)°K=	T(Substrt)=	P/A(Substrt)	P/A(Chip-N2)
0.1	0.7864558	0.8711601	0.7842378	0.04435851	0.05564149
0.15	0.9379986	1.06168	0.93476	0.06477047	0.08522952
0.2	1.061388	1.222649	1.057166	0.08445002	0.11555
0.25	1.167095	1.364789	1.161918	0.1035299	0.14647
0.3	1.260419	1.493572	1.254314	0.1220988	0.1779012
0.4	1.421278	1.722881	1.413381	0.1579452	0.2420548
0.5	1.558273	1.925572	1.548656	0.1923491	0.3076508
0.6	1.678627	2.109318	1.667349	0.2255469	0.3744532
0.7	1.786572	2.278674	1.773687	0.257707	0.4422931
0.8	1.884836	2.43661	1.870388	0.2889564	0.5110435
0.9	1.975292	2.585189	1.959323	0.3193948	0.5806053
1	2.059292	2.725917	2.041837	0.3491024	0.6508976
1.5	2.410968	3.3441	2.386534	0.4886687	1.011331
2	2.689357	3.866964	2.658522	0.6166969	1.383303
2.5	2.922789	4.328414	2.885983	0.7361069	1.763893
3	3.125354	4.745964	3.082919	0.8436913	2.151309
4	3.467538	5.487618	3.414643	1.057889	2.942111
5	3.752763	6.140816	3.690233	1.250591	3.749409
6	3.999181	6.730844	3.927654	1.430535	4.569465
7	4.217218	7.272824	4.137209	1.60018	5.39982
8	4.413473	7.776659	4.32541	1.761255	6.238745
9	4.59241	8.249254	4.496657	1.91504	7.08496
10	4.757204	8.695654	4.654078	2.062513	7.937487
11	4.910202	9.119678	4.799979	2.204446	8.795555

Figure 9

1mm MgO Substrate MCM, 3 mil Unloaded Epoxy Die Attach, 1-D Thermal Analysis with LN2 Pool Boiling (no subcooling or forced convection)



Horizontal is Chip Power Density in W/cm^2, Vertical is ΔT=T-Tsat [Tsat=77°K nom] for IC (Top), HTSC layers and Substrate (Bottom)

Figure 10

Summary of MgO Substrate MCMs with Various Epoxy Thicknesses

Calculation of HTSC Temperature vs. P/A In MCM with LN2 Nucleate Boiling R. C. Eden June 1991
1-D Calculation of HTSC ΔT in Nucleate Boiling LN2 Cooled MCM [ΔT=T-Tsat where Tsat=77°K nom].
Convective-Nucleate Xover @ ΔTX= .154292482034247 °K @ P/A= 1.332351724254022D-03 W/cm^2, without N2 subcooling.

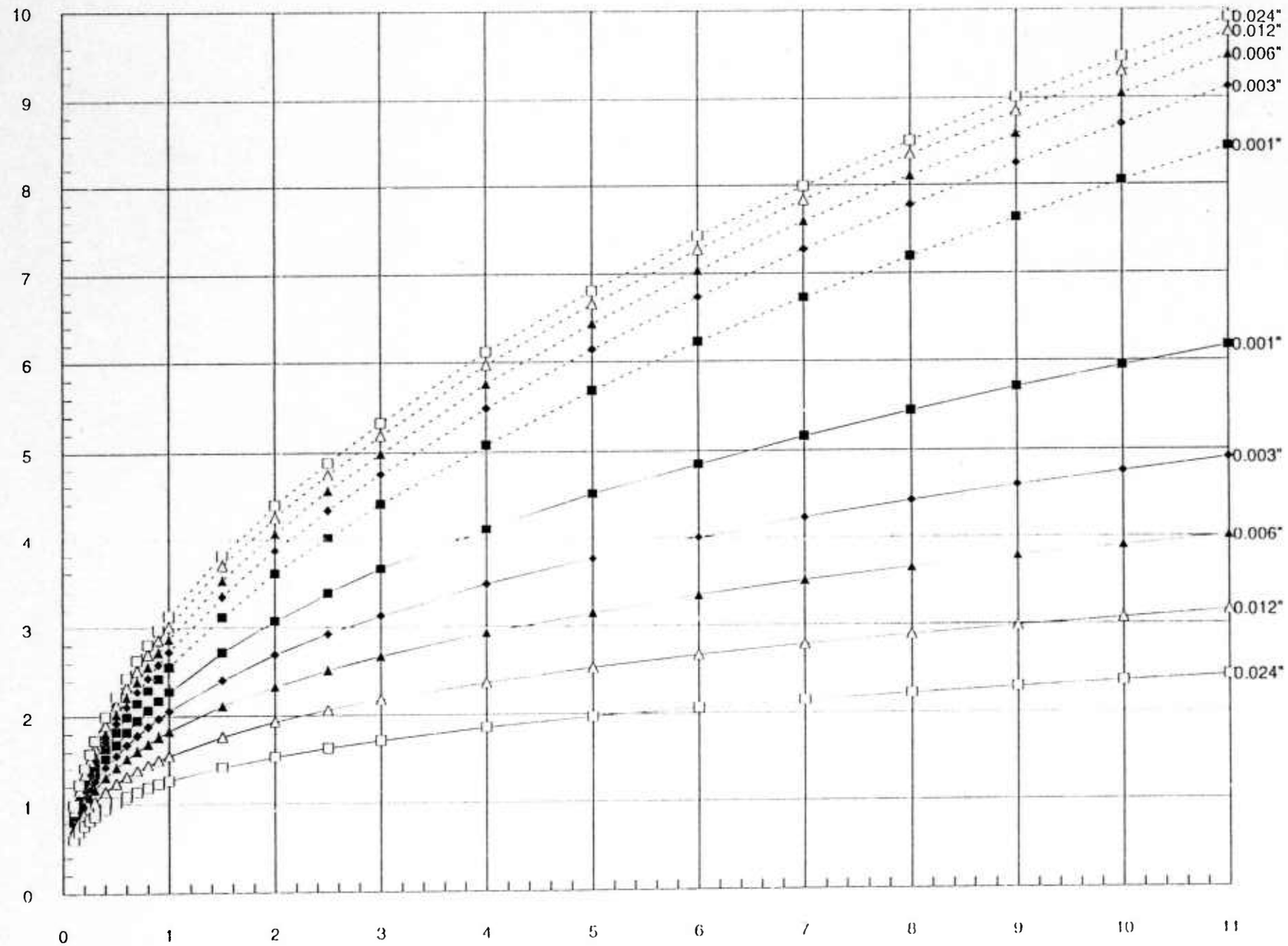
Thermal Conductivity of Epoxy Die Attach (e.g. 0.4W/m °K), KEPX= .4000000059604645
Thickness of Epoxy Die Attach in mils, Zepoxy= 1 (or 2.540005E-02 mm)
Si Chip Thickness, Zchip= .635 mm, Zsubstrate= 1 mm, Zepoxy= .001 inches

MCM Substrate Material is MgO with Thermal Conductivity of Ksub= 200 W/m°K
For 1 cm^2 area, the Thermal Resistances (in °K/W-cm^2) are:
RSI= 4.535714E-03 REPXY= .6350013 RSUB= .05 RTOT= .689537

	1 mil Unloaded Epoxy		3 mils Unloaded Epoxy		6 mil Epoxy		12 mils Epoxy		24 mils Epoxy	
P/A[W/cm^2]=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=	T(HTSC)°K=	T(chip)°K=
0.1	0.8147208	0.8453259	0.7864558	0.8711601	0.7495432	0.9021416	0.6904294	0.9460683	0.6081839	0.9972963
0.15	0.9792609	1.024696	0.9379986	1.06168	0.8856798	1.104097	0.8051799	1.160934	0.6986442	1.222934
0.2	1.115164	1.175216	1.061388	1.222649	0.9948175	1.275141	0.8954975	1.342533	0.768729	1.412622
0.25	1.232984	1.307471	1.167095	1.364789	1.087176	1.426345	0.9709023	1.502696	0.8266187	1.579233
0.3	1.338076	1.42684	1.260419	1.493572	1.167895	1.563395	1.036109	1.647536	0.8762864	1.729412
0.4	1.521593	1.638491	1.421278	1.722881	1.305337	1.807396	1.145809	1.904618	0.9591461	1.994965
0.5	1.680254	1.824799	1.558273	1.925572	1.420828	2.022908	1.236844	2.130856	1.027345	2.227749
0.6	1.821437	1.993203	1.678627	2.109318	1.521199	2.218057	1.315215	2.335085	1.085714	2.437269
0.7	1.949487	2.148094	1.786572	2.278674	1.610417	2.397698	1.384356	2.522585	1.136981	2.62918
0.8	2.067217	2.292319	1.884836	2.43661	1.691013	2.565009	1.446433	2.696812	1.182849	2.80717
0.9	2.176566	2.427847	1.975292	2.585189	1.764712	2.722206	1.502907	2.860174	1.22446	2.973799
1	2.278941	2.556107	2.059292	2.725917	1.832751	2.870909	1.554815	3.014431	1.262618	3.130931
1.5	2.716097	3.118888	2.410968	3.3441	2.113839	3.521939	1.767248	3.686981	1.418031	3.814065
2	3.071689	3.594863	2.689357	3.866964	2.332604	4.069883	1.930726	4.250097	1.536982	4.384157
2.5	3.376112	4.015425	2.922789	4.328414	2.513891	4.551567	2.065217	4.743344	1.634521	4.882476
3	3.64474	4.396609	3.125354	4.745964	2.659821	4.986024	2.180301	5.18705	1.7178	5.330094
4	4.107533	5.075546	3.467538	5.487618	2.930701	5.754792	2.37182	5.969944	1.856082	6.118721
5	4.501512	5.675763	3.752763	6.140816	3.146074	6.429168	2.529126	6.654806	1.96943	6.807651
6	4.847569	6.219863	3.999181	6.730844	3.33084	7.03646	2.663598	7.270316	2.06619	7.426239
7	5.157939	6.721292	4.217218	7.272824	3.493441	7.592932	2.781623	7.833471	2.15103	7.991824
8	5.440493	7.188825	4.413473	7.776659	3.639162	8.109198	2.887176	8.35532	2.26844	8.515652
9	5.700633	7.628569	4.59241	8.249254	3.771549	8.592635	2.982908	8.843518	2.29556	9.005498
10	5.942254	8.04498	4.757204	8.695654	3.893103	9.048618	3.070684	9.303627	2.358532	9.467005
11	6.168266	8.44143	4.910202	9.119678	4.005663	9.481205	3.151868	9.739835	2.416749	9.904416

Figure 11

Summary of 1mm MgO Substrate MCMs with 1, 3, 6, 12 and 24 mils Epoxy Die Attach Thickness, LN2 Pool Boiling w/o subcooling or forced convection



Horizontal is Chip Power Density in W/cm^2, Vertical is ΔT=T-Tsat [Tsat=77°K nom] for IC Chip (top) and HTSC Interconnects (Bottom)

Figure 12

Section 2.0

2.1. Application of Superconductivity to Motors and Generators

As a result of five visits and numerous conversations with American Superconductors Inc., we have concluded that this company (a) has a significant technology to offer and (b) has been completely by-passed as far as government R & D support is concerned. They have been totally supported by Venture Capital Funds. They have done an excellent job in training consortia with industry to supplement the V.C. funds. They have made significant progress towards application of their wires to the high and large motor market and promise to be in production within three years with a faculty of generic coils. Their initial customers (real) are the utilities. We have significant experience in this market niche and do believe we can help this company. The utility motor market can be significant and utilities have the incentives to use superconducting motors: energy saving and lower "effective cost". However these companies are conservative and follow-the-leader types. This means that American Superconductor must work with selected utility companies that play leadership roles, have the cash, and the R&D staff to develop and test these motors. To them reliability is a major issue. Should these "Leader" companies accept the Superconductivity technologies then the other hundreds of utilities will follow. We should like to highlight a major point: DARPA supports many universities and labs to research and few companies that will absorb and merchandize the superconductivity technology. Should American Superconductor go under, the question is this: What happens to the research; where is the outlet? It is important for DARPA to see to it that each R&D program has a smooth path to the merchant market. Generally speaking, R&D accomplishments that stall and do not get applied, get picked off by Japanese enterprises.

2.2. Superconducting MCM Technology

Several meetings took place with MIT, Cornell, Livermore, STI, Conductus, E-Systems, Cray, Datamax, and Carrier regarding the development of SC-MCM. Progress has been accomplished in program leadership, by bringing together the teams, and improving the confidence level in the film processing technology. However, more work meets to be done from a system overview. It is imperative that, since now it has become more clear that this technology has pay-offs, a more detailed look should be undertaken to better understand all system issues. Discussions with Datamax and Cray reveal that, indeed this technology can be exciting. but according to Tony Vacca of Cray, he likes to see a more in-depth system analysis done to insure that all issues are identified and prioritized. Towards that end we asked Loyd Thorndyke and Tony Vacca to detail their ideas in white paper and that in a few weeks, be ready to present them to E-Systems, DARPA, and Quad. We also encouraged both Cray and Datamax to visit the superconductivity vendors to get a feel for the film processing technology. We also recommend that soon after the start of the program. a review be held at Cray for the purpose of exchanging ideas. We think an early interaction with an end user can be very beneficial to all participants.

2.3. Passive μ-Wave Devices

As we mentioned in previous report this market niche is very small and will even get smaller as DOD budgets shrink. It behooves the superconductor vendors to understand this. Their only salvation is to vertically integrate and leverage their devices by selling front-ends. But they have little experience in this area. It seems to us that partnering with system houses may be a good idea. We therefore introduced STI to top management at E-Systems for the purpose of discussing this idea. Curtis Ritchie, V.P. of the Garland Division seems receptive to the idea and plans are underway to meet for this propose. It seems to us that this may give STI and Conductus an avenue to a somewhat larger market and a healthier stay until the MCM market begins.

2.4. Universities

We have interacted with several universities on the establishment of MCM curriculum so that students can be trained in MCM technology and be ready to contribute to the industry in a more opportune time.

2.5. Another MCM Team

Significant ground work has been done on the formation of another SC-MCM team should funds be available to kick it off.